


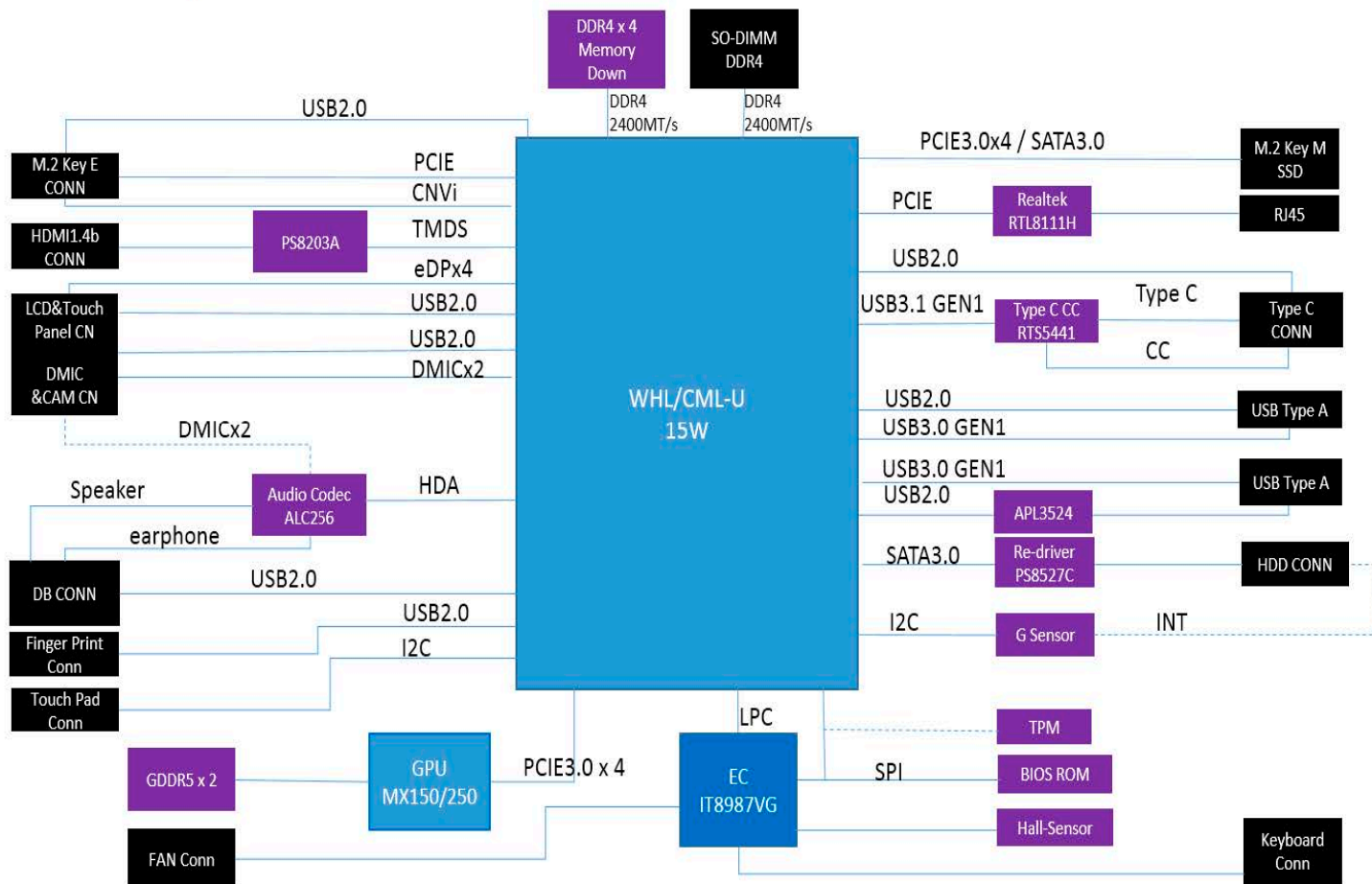
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Aspire5_NB8513_M/B Schematics Document Intel Whiskey Lake U-Processor with DDR4 REV3.0

2019-03-14

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Reviewer	Albert Zhou	Page name:	Cover page
Approver	Lobo Fan	Size: A4	Project Name: NB8513
		Date: Friday, March 22, 2019	REV: V1.0 Sheet: 1 of 72

EE MB Block Diagram



MEM ID

HW_ID0	HW_ID1	HW_ID2	Description	Total
0	0	0	4x Micron 8Gbx16 MT40A512M16TB-062E:J	4GB
1	0	0	4x Micron 8Gbx16 MT40A512M16LY-075:E	4GB
0	1	0	4x Hynix 8Gbx16 H5AN8G6NCJR-VKC	4GB
1	1	0	NA	NA
0	0	1	4x 16Gb(reserve)	8GB
1	0	1	4x 16Gb(reserve)	8GB
0	1	1	4x 16Gb(reserve)	8GB

GPU ID

HW_ID3	HW_ID4	Description
0	0	UMA
1	0	N17-G0
0	1	N17-G1
1	1	N17-G2

G-sensor ID

HW_ID5	Description
0	no g-sensor
1	G-sensor on board

FP ID

HW_ID6	Description
0	no FP
1	FP on board

TPM and fTPM ID

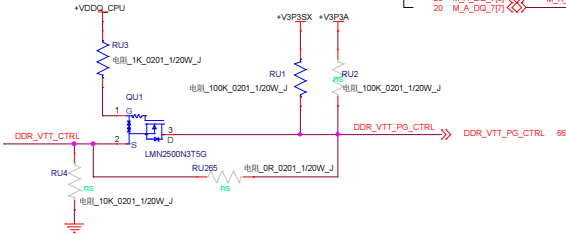
HW_ID7	Description
0	fTPM
1	TPM



CHA_SODIMM

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	20	M.A.DQ_0[1]	D29	DDR0_DQ_1DDR0_CK_1	V31	M.A_CK_DDR0_DP	
	20	M.A.DQ_0[2]	C28	DDR0_DQ_2DDR0_CK_2	V32	M.A_CK_DDR0_DP	
	20	M.A.DQ_0[3]	B27	DDR0_DQ_3DDR0_CK_3	V31	M.A_CK_DDR0_DP	
	20	M.A.DQ_0[4]	C28	DDR0_DQ_4DDR0_CK_4			
	20	M.A.DQ_0[5]	B27	DDR0_DQ_5DDR0_CK_5			
	20	M.A.DQ_0[6]	A28	DDR0_DQ_6DDR0_CK_6			
	20	M.A.DQ_0[7]	B27	DDR0_DQ_7DDR0_CK_7			
BYTE1	20	M.A.DQ_1[0]	C33	DDR0_DQ_8DDR0_CK_8			
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	20	M.A.DQ_1[2]	A32	DDR0_DQ_10DDR0_CK_10			
	20	M.A.DQ_1[3]	C33	DDR0_DQ_11DDR0_CK_11			
	20	M.A.DQ_1[4]	B33	DDR0_DQ_12DDR0_CK_12			
	20	M.A.DQ_1[5]	A32	DDR0_DQ_13DDR0_CK_13			
	20	M.A.DQ_1[6]	C33	DDR0_DQ_14DDR0_CK_14			
	20	M.A.DQ_1[7]	B33	DDR0_DQ_15DDR0_CK_15			
BYTE2	20	M.A.DQ_2[0]	H37	DDR0_DQ_16DDR0_CAB_0DDR0_MA_0			
	20	M.A.DQ_2[1]	H34	DDR0_DQ_17DDR0_CAB_1DDR0_MA_1			
	20	M.A.DQ_2[2]	K34	DDR0_DQ_18DDR0_CAB_2DDR0_MA_2			
	20	M.A.DQ_2[3]	K35	DDR0_DQ_19DDR0_CAB_3DDR0_MA_3			
	20	M.A.DQ_2[4]	H36	DDR0_DQ_20DDR0_CAB_4DDR0_MA_4			
	20	M.A.DQ_2[5]	H35	DDR0_DQ_21DDR0_CAB_5DDR0_MA_5			
	20	M.A.DQ_2[6]	K36	DDR0_DQ_22DDR0_CAB_6DDR0_MA_6			
	20	M.A.DQ_2[7]	K37	DDR0_DQ_23DDR0_CAB_7DDR0_MA_7			
BYTE3	20	M.A.DQ_3[0]	N34	DDR0_DQ_24DDR0_CAB_8DDR0_MA_8			
	20	M.A.DQ_3[1]	R37	DDR0_DQ_25DDR0_CAB_9DDR0_MA_9			
	20	M.A.DQ_3[2]	R34	DDR0_DQ_26DDR0_CAB_10DDR0_MA_10			
	20	M.A.DQ_3[3]	N37	DDR0_DQ_27DDR0_CAB_11DDR0_MA_11			
	20	M.A.DQ_3[4]	N35	DDR0_DQ_28DDR0_CAB_12DDR0_MA_12			
	20	M.A.DQ_3[5]	R36	DDR0_DQ_29DDR0_CAB_13DDR0_MA_13			
	20	M.A.DQ_3[6]	R35	DDR0_DQ_30DDR0_CAB_14DDR0_MA_14			
	20	M.A.DQ_3[7]	A35	DDR0_DQ_31DDR0_CAB_15DDR0_MA_15			
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	20	M.A.DQ_4[1]	A34	DDR0_DQ_33DDR0_CAB_17DDR0_MA_17			
	20	M.A.DQ_4[2]	A33	DDR0_DQ_34DDR0_CAB_18DDR0_MA_18			
	20	M.A.DQ_4[3]	A32	DDR0_DQ_35DDR0_CAB_19DDR0_MA_19			
	20	M.A.DQ_4[4]	A31	DDR0_DQ_36DDR0_CAB_20DDR0_MA_20			
	20	M.A.DQ_4[5]	A30	DDR0_DQ_37DDR0_CAB_21DDR0_MA_21			
	20	M.A.DQ_4[6]	A29	DDR0_DQ_38DDR0_CAB_22DDR0_MA_22			
	20	M.A.DQ_4[7]	A28	DDR0_DQ_39DDR0_CAB_23DDR0_MA_23			
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	20	M.A.DQ_5[2]	A33	DDR0_DQ_42DDR0_DQSP_2DDR0_DQSP_2			
	20	M.A.DQ_5[3]	A32	DDR0_DQ_43DDR0_DQSP_3DDR0_DQSP_3			
	20	M.A.DQ_5[4]	A31	DDR0_DQ_44DDR0_DQSP_4DDR0_DQSP_4			
	20	M.A.DQ_5[5]	A30	DDR0_DQ_45DDR0_DQSP_5DDR0_DQSP_5			
	20	M.A.DQ_5[6]	A29	DDR0_DQ_46DDR0_DQSP_6DDR0_DQSP_6			
	20	M.A.DQ_5[7]	A28	DDR0_DQ_47DDR0_DQSP_7DDR0_DQSP_7			
BYTE6	20	M.A.DQ_6[0]	B33	DDR0_DQ_48DDR0_DQSP_8DDR0_DQSP_8			
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	20	M.A.DQ_6[2]	B35	DDR0_DQ_50DDR0_DQSP_10DDR0_DQSP_10			
	20	M.A.DQ_6[3]	B36	DDR0_DQ_51DDR0_DQSP_11DDR0_DQSP_11			
	20	M.A.DQ_6[4]	B37	DDR0_DQ_52DDR0_DQSP_12DDR0_DQSP_12			
	20	M.A.DQ_6[5]	B38	DDR0_DQ_53DDR0_DQSP_13DDR0_DQSP_13			
	20	M.A.DQ_6[6]	B39	DDR0_DQ_54DDR0_DQSP_14DDR0_DQSP_14			
	20	M.A.DQ_6[7]	B40	DDR0_DQ_55DDR0_DQSP_15DDR0_DQSP_15			
BYTE7	20	M.A.DQ_7[0]	B41	DDR0_DQ_56DDR0_DQSP_16DDR0_DQSP_16			
	20	M.A.DQ_7[1]	B42	DDR0_DQ_57DDR0_DQSP_17DDR0_DQSP_17			
	20	M.A.DQ_7[2]	B43	DDR0_DQ_58DDR0_DQSP_18DDR0_DQSP_18			
	20	M.A.DQ_7[3]	B44	DDR0_DQ_59DDR0_DQSP_19DDR0_DQSP_19			
	20	M.A.DQ_7[4]	B45	DDR0_DQ_60DDR0_DQSP_20DDR0_DQSP_20			
	20	M.A.DQ_7[5]	B46	DDR0_DQ_61DDR0_DQSP_21DDR0_DQSP_21			
	20	M.A.DQ_7[6]	B47	DDR0_DQ_62DDR0_DQSP_22DDR0_DQSP_22			
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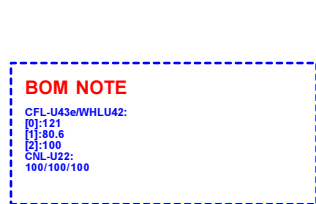
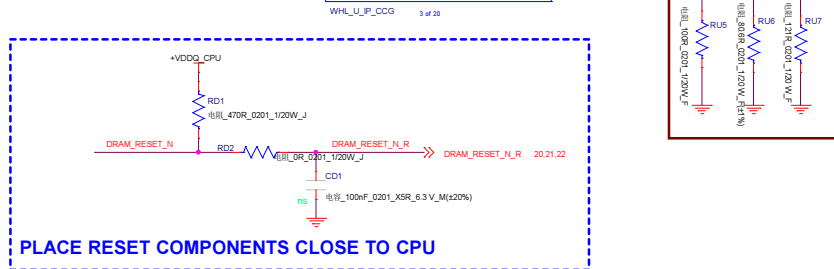
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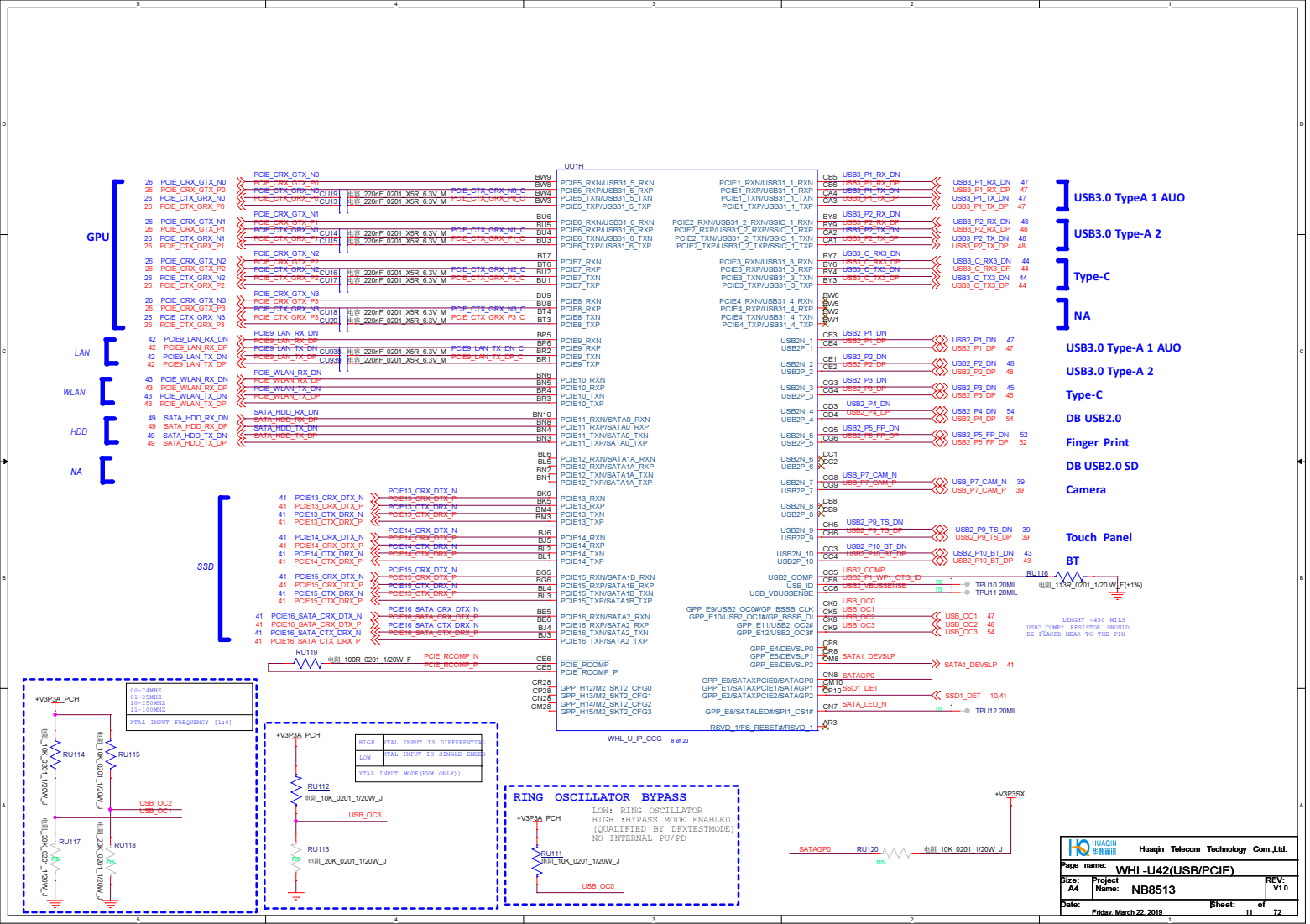


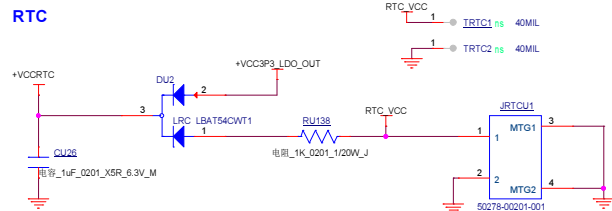
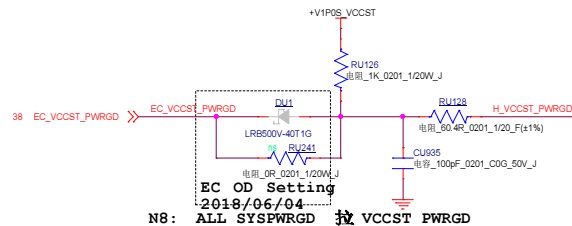
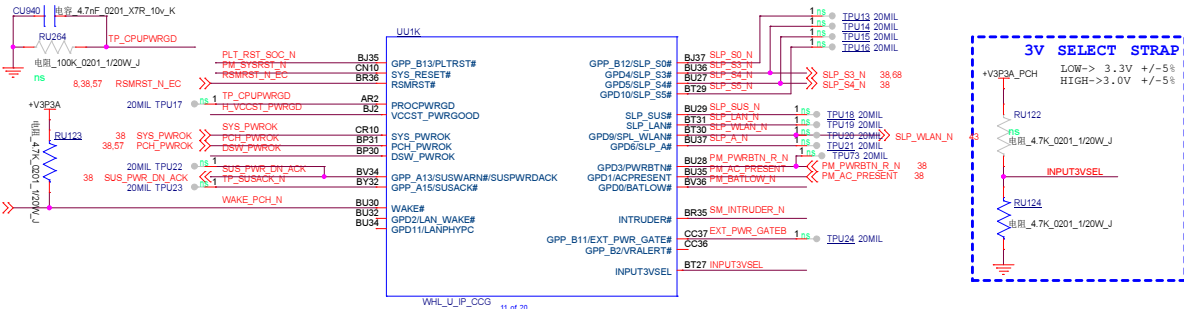
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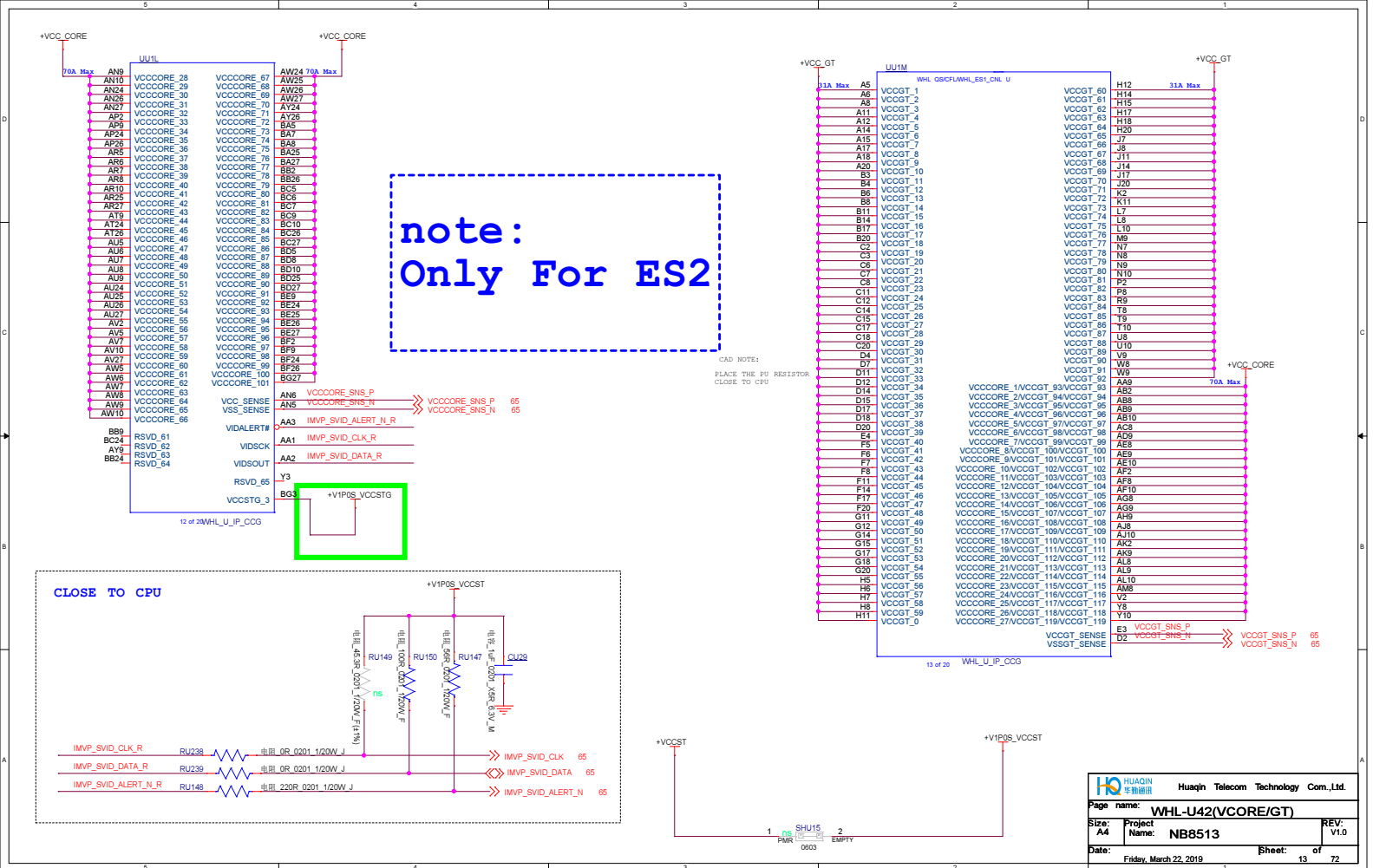
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	21	M_B_DQ_01	R25	DOR1_DQ_10DOR0_DQ_10DOR1_CKP_0DOR1_CKP_0	AF28 M_B_CK_DDR0_DP
	21	M_B_DQ_02	R22	DOR1_DQ_20DOR0_DQ_20DOR1_CKN_1DOR1_CKN_1	AF28 M_B_CK_DDR0_DN
	21	M_B_DQ_03	R25	DOR1_DQ_30DOR0_DQ_30DOR1_CKP_1DOR1_CKP_1	AF28 M_B_CK_DDR0_DP
	21	M_B_DQ_04	R22	DOR1_DQ_40DOR0_DQ_40	T28 M_B_CKED
	21	M_B_DQ_05	R25	DOR1_DQ_50DOR0_DQ_50DOR1_CKE_0DOR1_CKE_0	T28 M_B_CKED
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BYTE1	21	M_B_DQ_08	R22	DOR1_DQ_80DOR0_DQ_80DOR1_CKE_3DOR1_CKE_3	T28 M_B_CKED
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	21	M_B_DQ_10	R22	DOR1_DQ_100DOR0_DQ_100DOR1_CKE_5DOR1_CKE_5	T28 M_B_CKED
	21	M_B_DQ_11	R25	DOR1_DQ_110DOR0_DQ_110DOR1_CKE_6DOR1_CKE_6	T28 M_B_CKED
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	21	M_B_DQ_13	R25	DOR1_DQ_130DOR0_DQ_130DOR1_CKE_8DOR1_CKE_8	T28 M_B_CKED
	21	M_B_DQ_14	R22	DOR1_DQ_140DOR0_DQ_140DOR1_CKE_9DOR1_CKE_9	T28 M_B_CKED
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	21	M_B_DQ_25	R25	DOR1_DQ_250DOR0_DQ_250DOR1_CKE_20DOR1_CKE_20	T28 M_B_CKED
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	21	M_B_DQ_31	R25	DOR1_DQ_310DOR0_DQ_310DOR1_CKE_26DOR1_CKE_26	T28 M_B_CKED
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BYTE5	21	M_B_DQ_40	R22	DOR1_DQ_400DOR0_DQ_400DOR1_CKE_35DOR1_CKE_35	T28 M_B_CKED
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	21	M_B_DQ_42	R22	DOR1_DQ_420DOR0_DQ_420DOR1_CKE_37DOR1_CKE_37	T28 M_B_CKED
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BYTE6	21	M_B_DQ_48	R22	DOR1_DQ_480DOR0_DQ_480DOR1_CKE_43DOR1_CKE_43	T28 M_B_CKED
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BYTE7	21	M_B_DQ_56	R22	DOR1_DQ_560DOR0_DQ_560DOR1_CKE_51DOR1_CKE_51	T28 M_B_CKED
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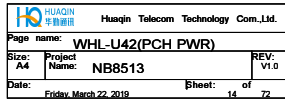
1.change RU7 to 121Ω 2018 08 06

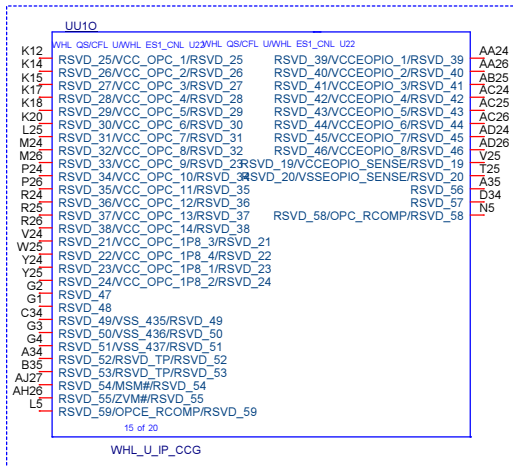
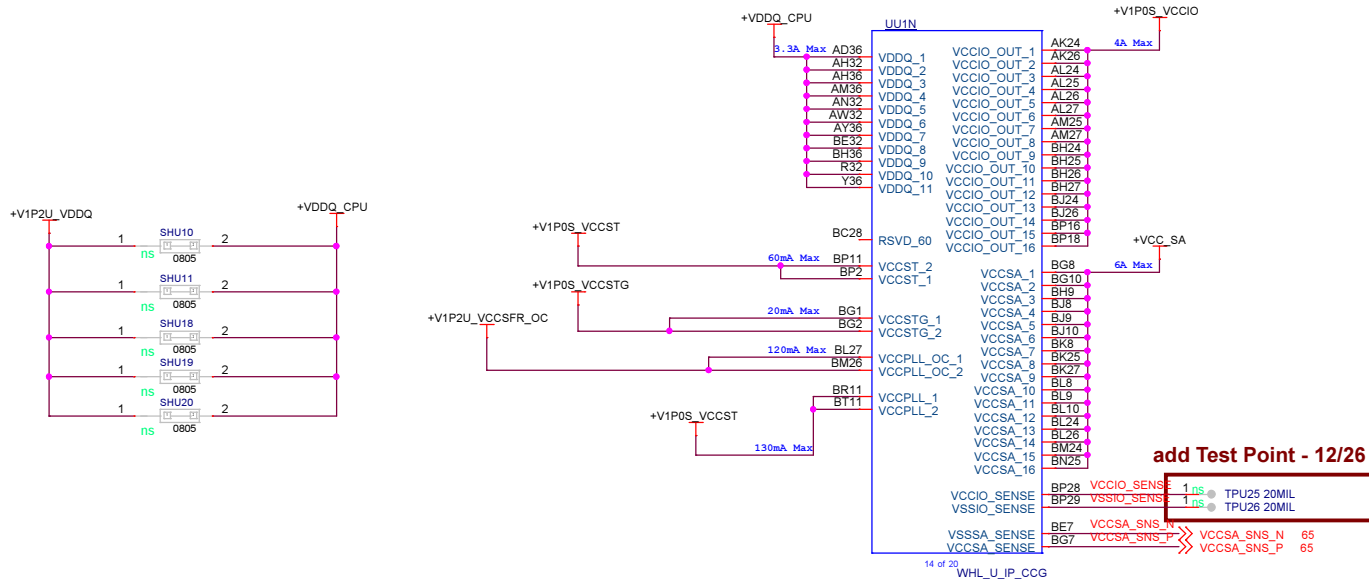












LU1R

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B16	VSS_361	VSS_330	AE26
BY5	VSS_361	VSS_337	BU33
CP18	VSS_361	VSS_345	CV16
CU37	VSS_371	VSS_364	AE27
CK37	VSS_381	VSS_364	BU35
AV11	VSS_381	VSS_374	CH13
CM1	VSS_401	VSS_384	AE30
BO5	VSS_411	VSS_380	CH13
AY4	VSS_421	VSS_388	CH13
B34	VSS_370	VSS_322	AE27
E36	VSS_380	VSS_329	CH17
AE4	VSS_390	VSS_336	CH17
AE26	VSS_400	VSS_344	BN30
AF25	VSS_410	VSS_353	AF14
AG24	VSS_420	VSS_363	AF14
AG26	VSS_428	VSS_373	BN17
AI14	VSS_434	VSS_386	CH15
AH26	VSS_296	VSS_301	AF30
B2	VSS_360	VSS_307	CH29
B36	VSS_369	VSS_314	AF33
C37	VSS_389	VSS_321	BP16
C36	VSS_379	VSS_328	AF36
CH1	VSS_389	VSS_336	AF4
CH2	VSS_409	VSS_362	CH5
CU39	VSS_419	VSS_362	AF7
CP2	VSS_427	VSS_416	BP26
D1	VSS_433	VSS_426	CH6
A32	VSS_341	VSS_433	AG10
F33	VSS_349	VSS_294	BP3
A3	VSS_358	VSS_300	CP11
CU36	VSS_368	VSS_306	BP30
A36	VSS_378	VSS_313	AH27
BK10	VSS_388	VSS_320	BP33
CL14	VSS_388	VSS_327	CP13
AB27	VSS_418	VSS_405	AH28
BK4	VSS_426	VSS_416	BP4
CK1	VSS_433	VSS_424	CP16
AB3	VSS_340	VSS_431	BP7
BP28	VSS_348	VSS_393	AI30
AB30	VSS_367	VSS_399	CP18
BK3	VSS_367	VSS_305	CP21
AE33	VSS_377	VSS_312	AI31
BK33	VSS_387	VSS_319	BR19
CKV	VSS_407	VSS_384	CP27
AE36	VSS_417	VSS_404	AI33
BK4	VSS_426	VSS_414	BP25
IL1	VSS_332	VSS_423	AI35
AB4	VSS_339	VSS_430	CP37
BK7	VSS_347	VSS_392	AI35
CU13	VSS_356	VSS_388	AJ28
AB7	VSS_368	VSS_394	BI16
BL26	VSS_376	VSS_311	CP9
CU17	VSS_386	VSS_318	CP2
BL28	VSS_396	VSS_383	CH2
CM21	VSS_406	VSS_383	AH3
A-22	VSS_417	VSS_403	CH36
BL29	VSS_324	VSS_413	AH33
CM26	VSS_331	VSS_422	D21
AC36	VSS_338	VSS_429	AF36
BL30	VSS_346	VSS_291	BP1
CU28	VSS_355	VSS_297	BI25
BL31	VSS_365	VSS_303	AH4
CM31	VSS_375	VSS_310	BT28
AD33	VSS_385	VSS_372	AL28
BL32	VSS_395	VSS_382	AL28
CM33	VSS_399	VSS_382	BI33
AD36	VSS_316	VSS_402	AL29
	VSS_323	VSS_412	VSS_278

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WHL_U_IP_CCG

LU1S

BT35	VSS_277	VSS_181	BY25
AL32	VSS_290	VSS_183	AU32
BY38	VSS_158	VSS_186	BY29
D8	VSS_165	VSS_245	J21
AL1	VSS_172	VSS_253	BY35
AL1	VSS_208	VSS_271	AV25
AM10	VSS_217	VSS_284	J24
BU11	VSS_238	VSS_161	BY36
E23	VSS_238	VSS_161	BY36
AM25	VSS_263	VSS_175	AV33
E27	VSS_263	VSS_175	BY36
AM33	VSS_276	VSS_177	AV33
BU23	VSS_289	VSS_185	AV33
E39	VSS_155	VSS_233	AV33
AM35	VSS_164	VSS_244	AV36
BU24	VSS_200	VSS_254	AV36
E31	VSS_207	VSS_269	C1
BU25	VSS_216	VSS_281	C1
E33	VSS_228	VSS_150	AV4
AN25	VSS_237	VSS_168	C21
BU1	VSS_249	VSS_168	C21
E9	VSS_262	VSS_174	AV8
AM28	VSS_154	VSS_233	C26
BY11	VSS_288	VSS_222	K24
F12	VSS_194	VSS_243	AV8
AN29	VSS_189	VSS_239	C26
P15	VSS_206	VSS_259	AV28
AV33	VSS_215	VSS_283	C33
F18	VSS_225	VSS_148	AW28
BU3	VSS_236	VSS_159	K27
F33	VSS_248	VSS_167	C4
F7	VSS_261	VSS_173	C4
BY31	VSS_274	VSS_212	AW3
F21	VSS_287	VSS_221	C8
AN8	VSS_189	VSS_231	C38
F24	VSS_193	VSS_244	AW30
BY33	VSS_198	VSS_254	CA11
F24	VSS_205	VSS_267	K3
BY4	VSS_214	VSS_281	AW21
F3	VSS_224	VSS_148	CA15
AP5	VSS_235	VSS_159	CA15
BU11	VSS_247	VSS_168	AY33
AP33	VSS_260	VSS_203	CA22
BU15	VSS_273	VSS_211	K27
Q21	VSS_185	VSS_220	AY35
AP36	VSS_188	VSS_238	AY35
Q27	VSS_162	VSS_241	C32
AP4	VSS_197	VSS_253	K4
Q33	VSS_204	VSS_266	BI13
AP28	VSS_213	VSS_280	CA25
Q36	VSS_234	VSS_147	BI16
C36	VSS_234	VSS_151	BI16
AT33	VSS_248	VSS_196	CB11
AW21	VSS_259	VSS_200	J27
G9	VSS_272	VSS_210	B21
AT36	VSS_198	VSS_218	BI18
H21	VSS_153	VSS_223	B33
AT36	VSS_248	VSS_241	B36
BVO	VSS_176	VSS_251	B36
H27	VSS_177	VSS_265	CB18
AT1	VSS_181	VSS_181	CB19
BY11	VSS_184	VSS_148	B27
AU10	VSS_192	VSS_192	CB19
BY15	VSS_191	VSS_195	L6
H9	VSS_258	VSS_201	B29
AU28	VSS_271	VSS_208	BY29
BY22	VSS_285	VSS_218	Y25
J12	VSS_152	VSS_223	BY30
AL29	VSS_162	VSS_238	B31
J15	VSS_170	VSS_251	CB30
	VSS_176	VSS_264	N27
			CB35

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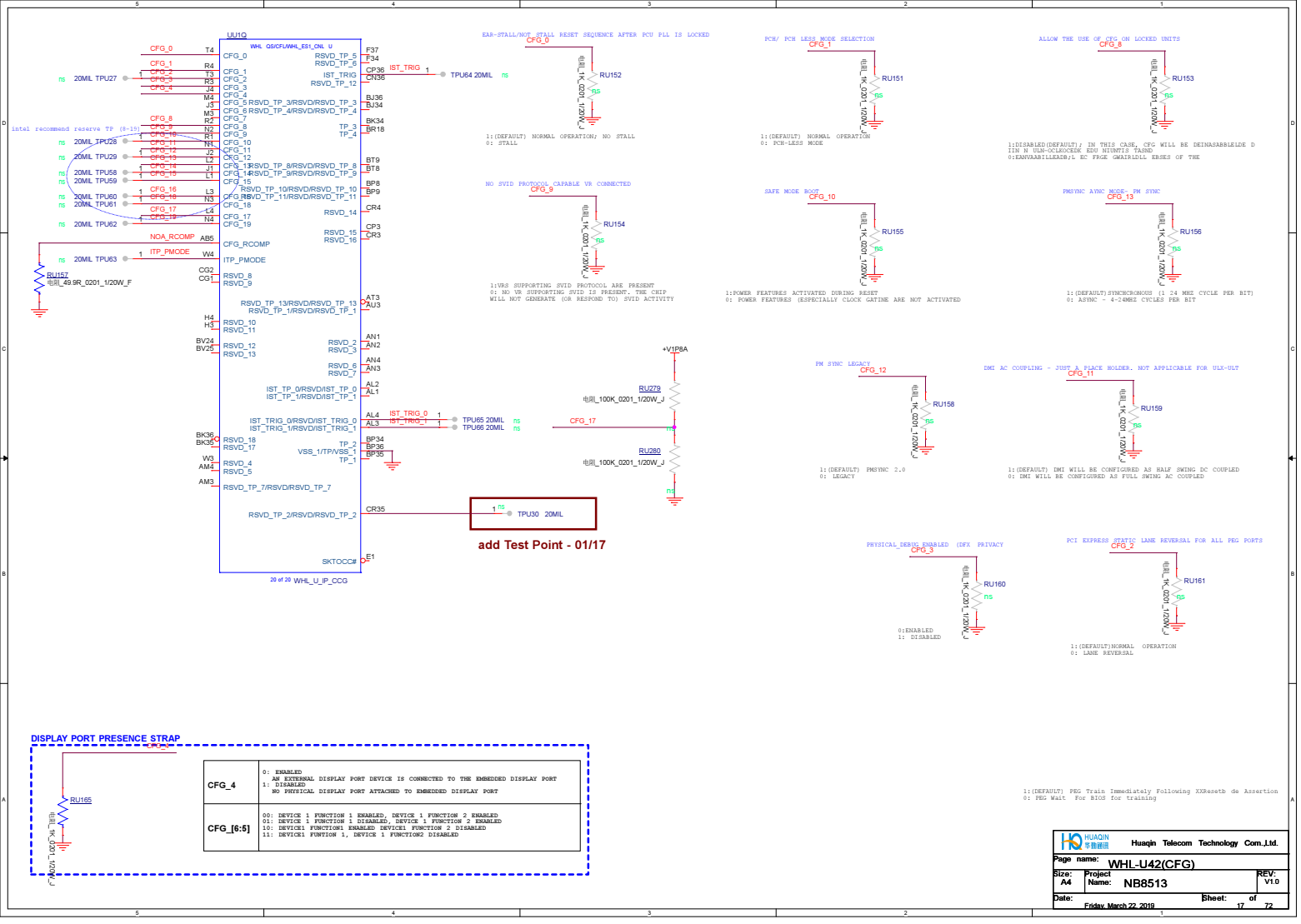
WHL_U_IP_CCG

LU1T

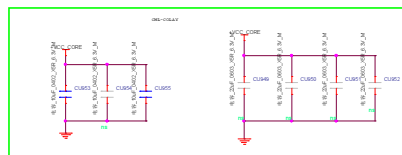
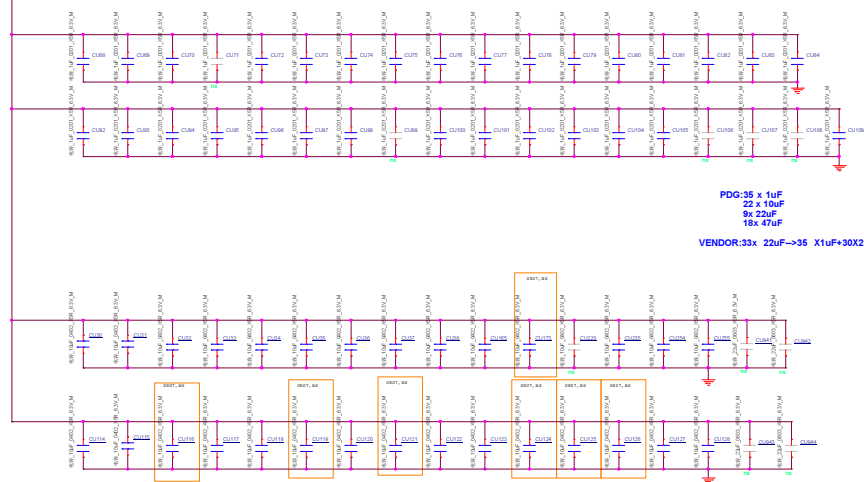
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B37	VSS_73	VSS_100	BE30
CB1	VSS_79	VSS_115	BE30
P10	VSS_84	VSS_126	W10
CB31	VSS_89	VSS_139	BE31
B5	VSS_96	VSS_8	CF3
B7	VSS_102	VSS_19	CF7
CB4	VSS_110	VSS_29	CF7
P33	VSS_120	VSS_83	W30
B9	VSS_132	VSS_87	W30
CB7	VSS_145	VSS_92	CG33
P36	VSS_14	VSS_114	BE33
BA10	VSS_26	VSS_106	W37
CH11	VSS_44	VSS_114	CG7
F4	VSS_52	VSS_138	W38
BA28	VSS_52	VSS_138	W38
F7	VSS_65	VSS_18	BE1
BA1	VSS_65	VSS_18	CH51
CB21	VSS_72	VSS_27	W37
R27	VSS_76	VSS_82	CF3
BE3	VSS_131	VSS_86	Y30
CB22	VSS_144	VSS_81	BE31
P28	VSS_13	VSS_87	CH11
BE35	VSS_24	VSS_104	CB33
BB33	VSS_34	VSS_113	V33
R29	VSS_43	VSS_124	Y35
BB35	VSS_51	VSS_137	BE28
PC31	VSS_58	VSS_6	CH19
R30	VSS_54	VSS_70	Y7
BE1	VSS_71	VSS_76	BP29
CC7	VSS_119	VSS_81	CH23
K31	VSS_130	VSS_85	BE33
BC25	VSS_143	VSS_90	CH28
K33	VSS_12	VSS_26	CH35
CD11	VSS_23	VSS_103	BE33
CD12	VSS_33	VSS_112	BE35
T30	VSS_42	VSS_12	CH35
BC29	VSS_50	VSS_136	BP19
CD14	VSS_57	VSS_1	VSS1
BK3	VSS_63	VSS_17	BE18
T35	VSS_109	VSS_82	BY19
BC39	VSS_118	VSS_48	CH34
CD24	VSS_129	VSS_47	BU18
T39	VSS_142	VSS_61	CH34
CD29	VSS_11	VSS_82	BR22
T7	VSS_32	VSS_76	BU20
CE33	VSS_41	VSS_80	BT14
U29	VSS_46	VSS_135	BP17
BO28	VSS_56	VSS_4	CH74
CE35	VSS_101	VSS_15	BE1
UV	VSS_108	VSS_2	CC24
BO33	VSS_117	VSS_37	U24
CE36	VSS_128	VSS_46	BE1
V26	VSS_141	VSS_54	AR4
BO35	VSS_145	VSS_10	AU4
CE7	VSS_21	VSS_68	AW4
V27	VSS_31	VSS_74	BA5
BO36	VSS_40	VSS_122	CH3
CF11	VSS_48	VSS_134	BE4
BE10	VSS_94	VSS_34	BE3
BE10	VSS_100	VSS_15	BE3
CF14	VSS_107	VSS_26	BE3
V30	VSS_116	VSS_39	BE3
BE28	VSS_127	VSS_45	CH2
CF18	VSS_140	VSS_105	CH2
V43	VSS_9	VSS_80	AW2
BE29	VSS_20	VSS_87	CM4
CF1	VSS_30	VSS_111	AC5
V36	VSS_39	VSS_121	AG5
BE3	VSS_98	VSS_135	CH6
	VSS_93	VSS_2	

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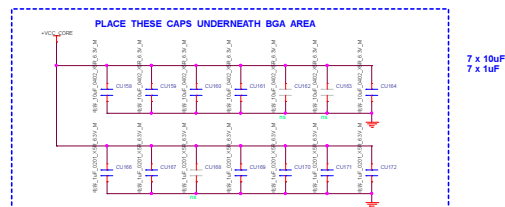
WHL_U_IP_CCG



+VCCGT



+VCCEOPIO delete

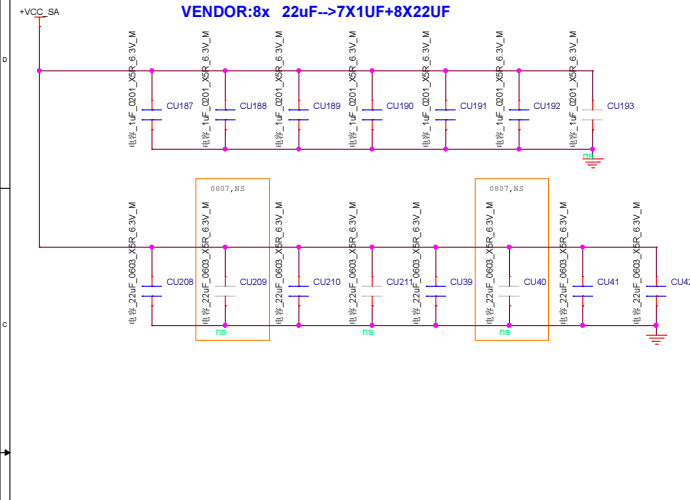


PDG:15 x 10uF
11 x 1uF
15 x 22uF
8 x 47uF
7x(0603)
2x(0805)

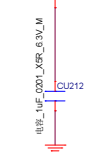
VENDOR:26x 22uF-->11X1uF+26x 22uF

PDG:7x 1uF
15X 10uF
2 x 47 uF
2 x (0805)

VENDOR:8x 22uF-->7X1UF+8X22UF

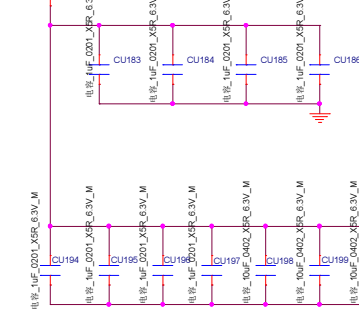


+V1P2U_VCCSFR_OC



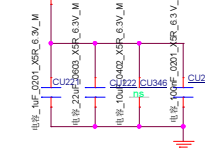
VCCPLL-OC 1x1uF

+V1P0S_VCCIO



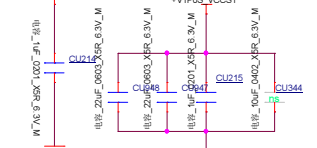
VCCPLL 1x1uF,1X0.1,2X(0402 10uF)

+V1P0S_VCCST



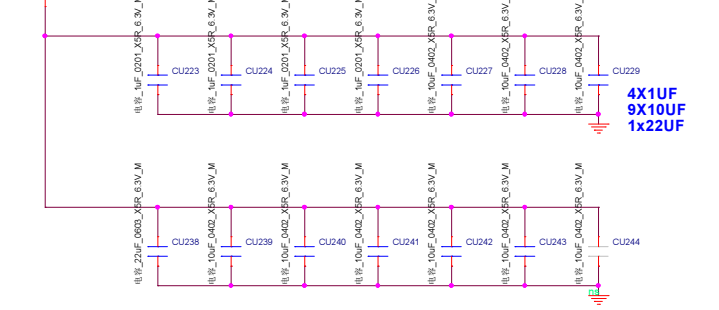
VCCSTG 1x1uF

+V1P0S_VCCSTG



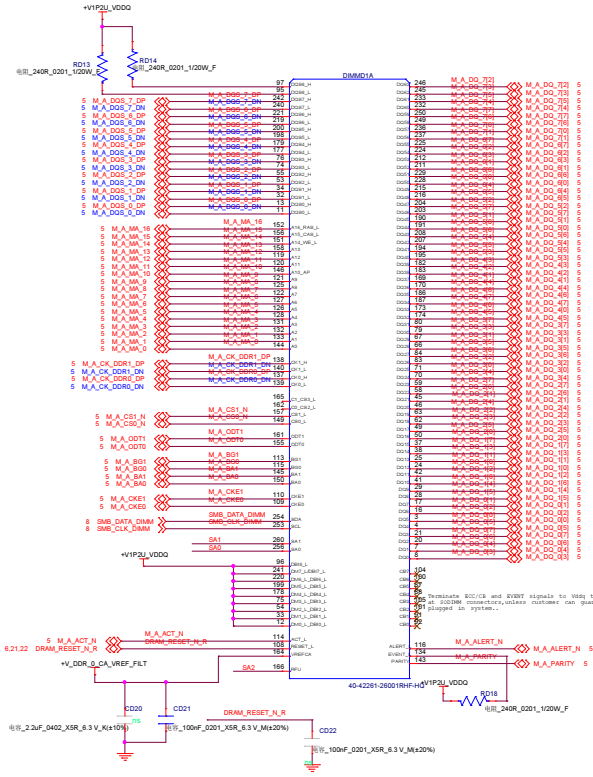
VCCST 1x1uF

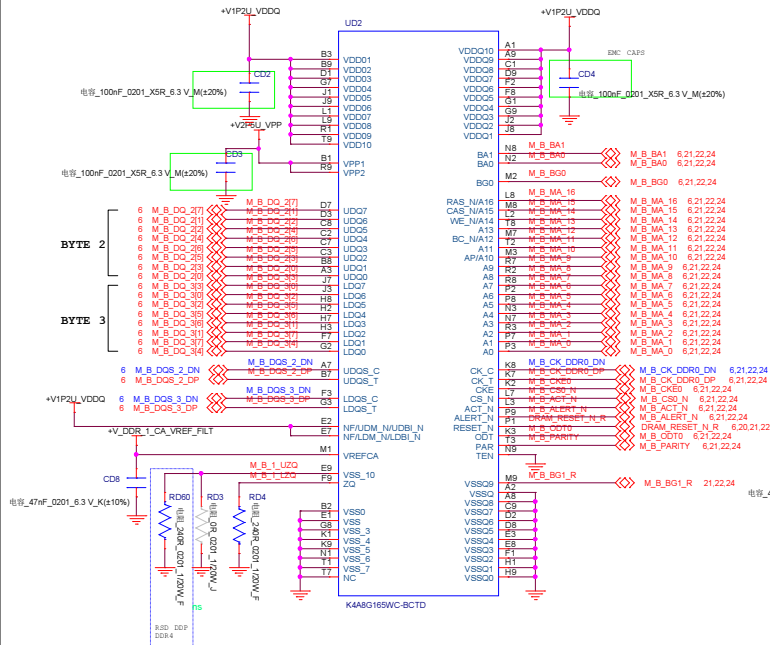
+VDDq_CPU



4X1UF
9X10UF
1x22UF

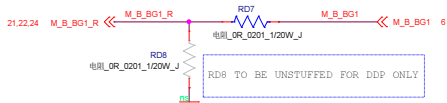
8X 1uF
6X10UF
4x(0402)





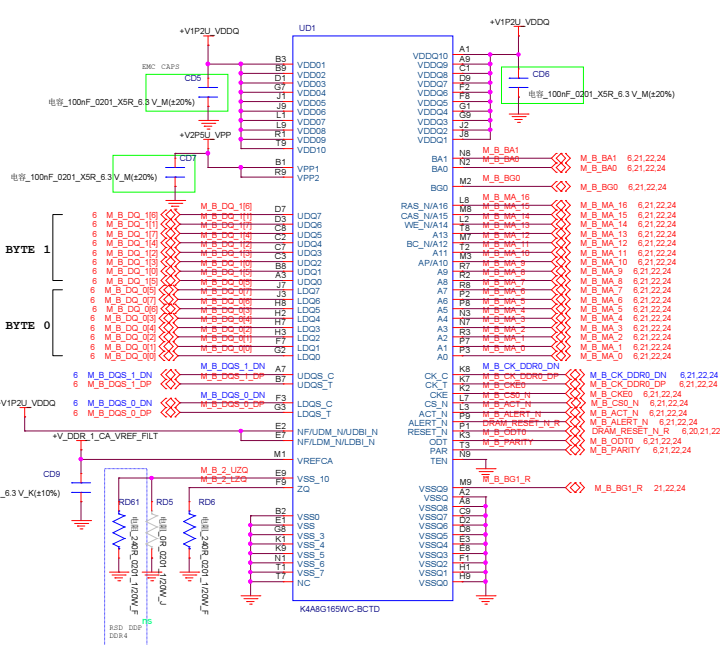
NOTE: TO BE STUFF FOR DUAL ZQ PARTS

RD7 TO BE STUFFED FOR DDP ONLY

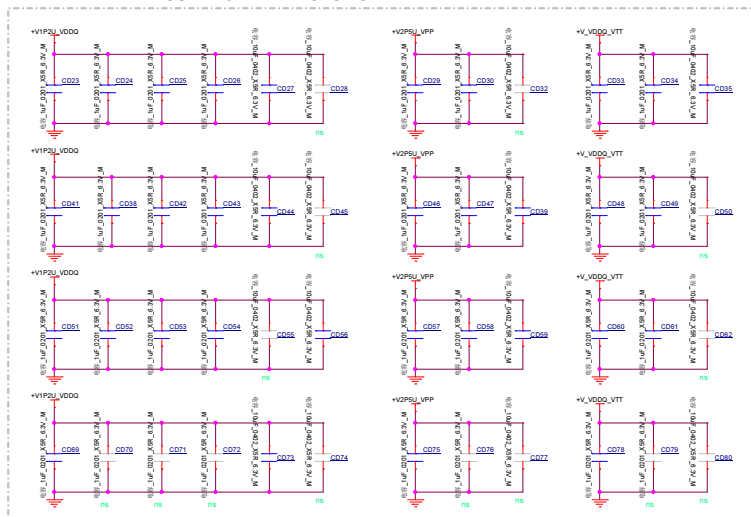


BOM NOTE

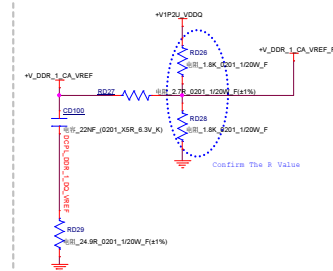
DDR PINS	SDP	DDP
E8	UZQ	GND
M8	BG1	GND
		BG1 SIG FROM CONTROLLER



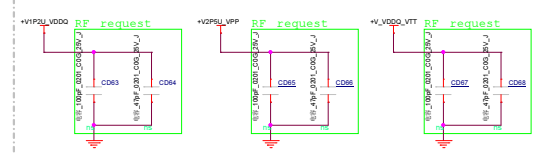
DECOUPLING CAPACITORS FOR DDR CHANNEL B MD



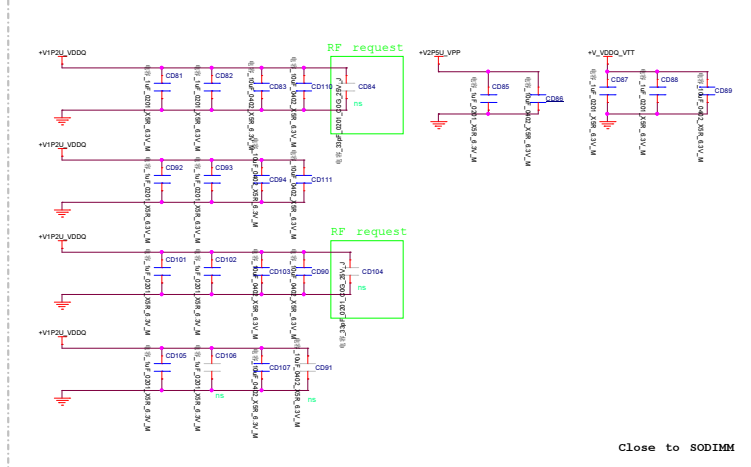
DDR CH B MD REF GENERATION



CHB MD

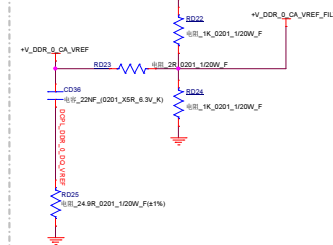


DECOUPLING CAPACITORS FOR DDR CHANNEL A SODIMM



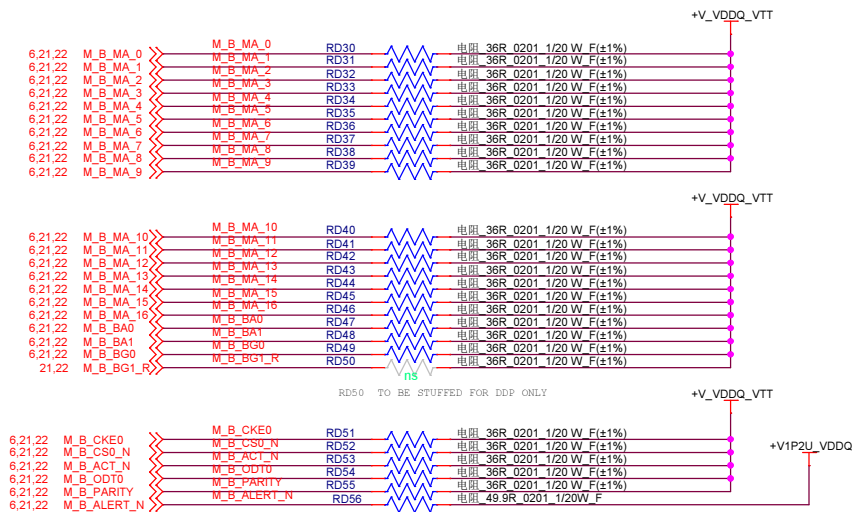
Close to SODIMM

DDR CH A SODIMM REF GENERATION

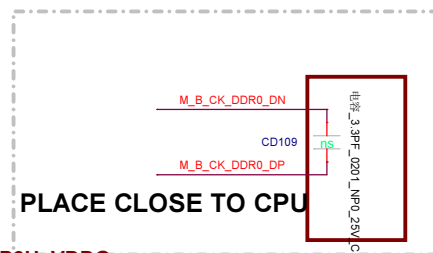
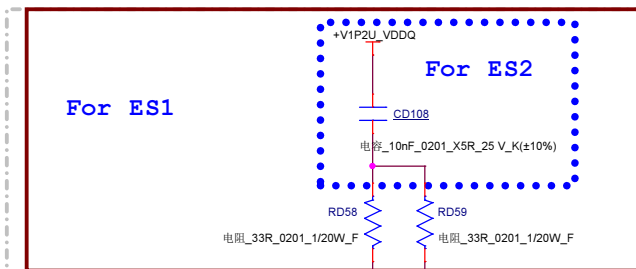


MEMORY TERMINATIONS

CHANNEL B MD



RD50 TO BE STUFFED FOR DDP ONLY




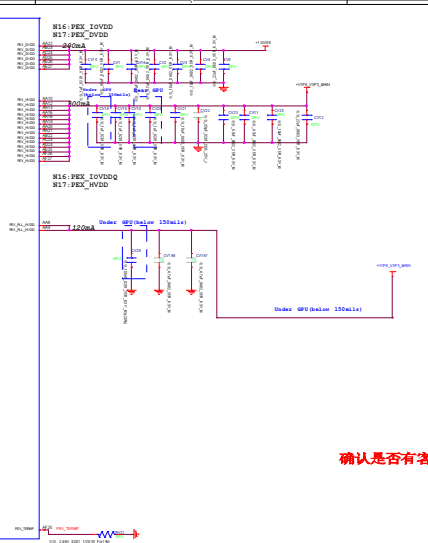
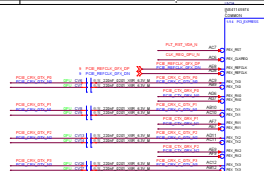
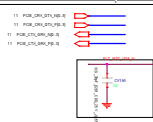
- 1.change +V VDDQ_VTT to +V1P2U_VDDQ
2. add CAP CD155 for ES2 sample - 01/04
3. add RD89 for ES1 sample -01/23

change CD146 to 3.3pF - 01/04

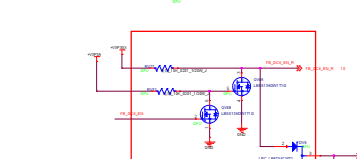
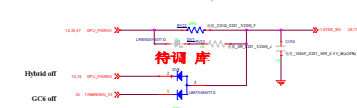
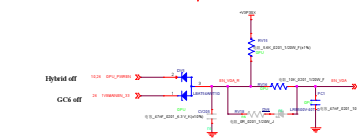
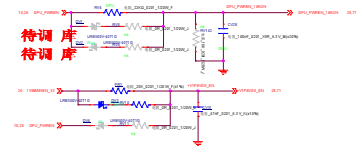
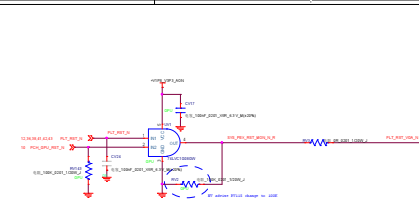
PLACE TERMINATION RESISTOR CLOSE TO LAST CHIP



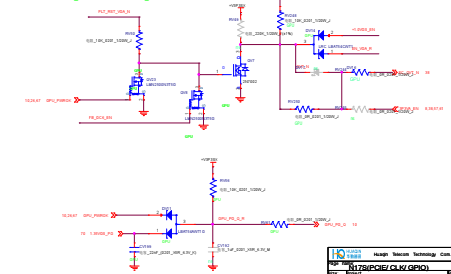
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Date:	Friday, March 22, 2019		Sheet: 25 of 72

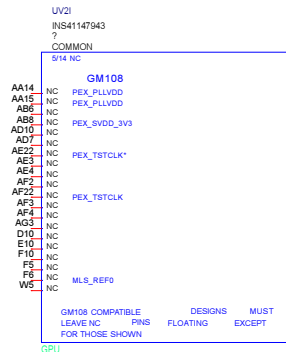
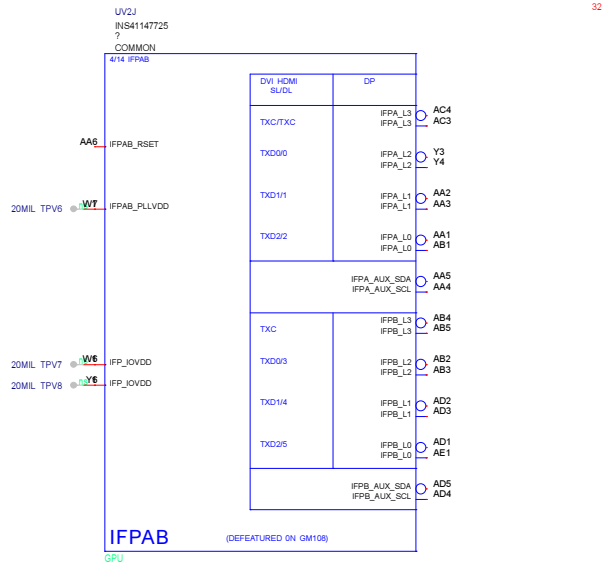
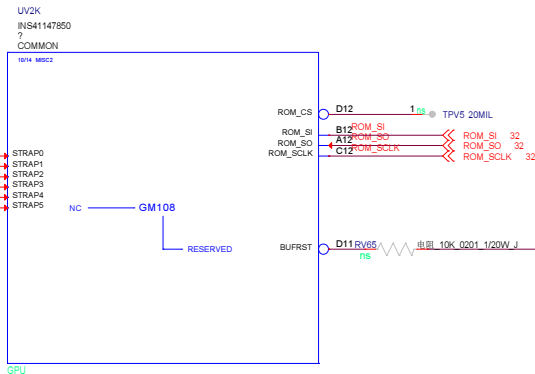
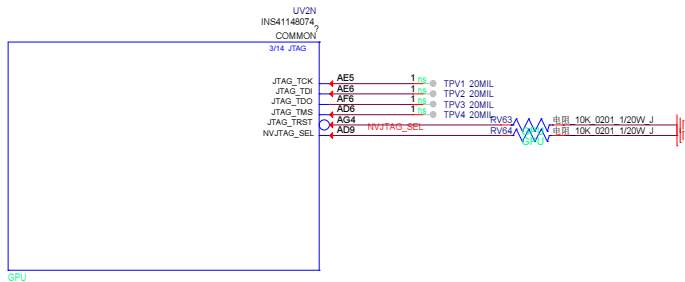


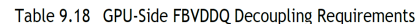
确认是否有客 供料料号



GPU core power loopback shutdown







FBVDDQ Decoupling Requirements		
	Recommended Quantity and Placement (for all supported partitions combined)	
Package Size	Quantity	Placement
GB2C-64 (preliminary)		
X65 [0402]	8	Under GPU FBVDDQ ball (evenly distributed throughout partition)
X65 [0603]	3	
X65 [0603]	1	Near GPU device
X65 [0603]	3	
GB4-128 (preliminary)		
X65 [0402]	12	Under GPU FBVDDQ ball (equally distributed across partitions)
X65 [0603]	4	
X65 [0603]	2	Near GPU device
X65 [0603]	5	
GB4-256		
X65 [0402]	24	Under GPU FBVDDQ ball (equally distributed across partitions)
X65 [0603]	5	
X65 [0603]	7	Near GPU device
X65 [0603]	9	

Move to Power Page 2018/06/07

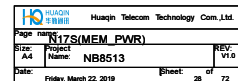


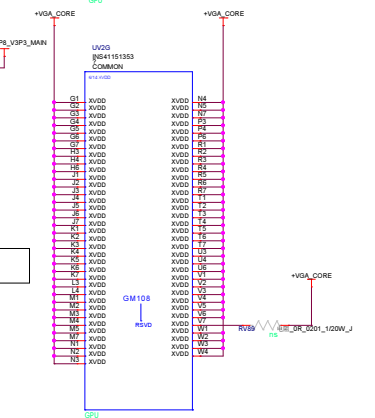
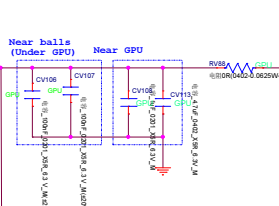
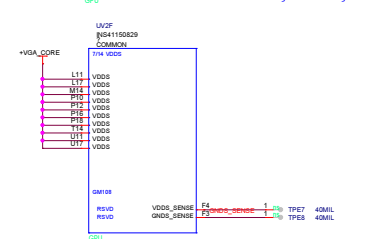
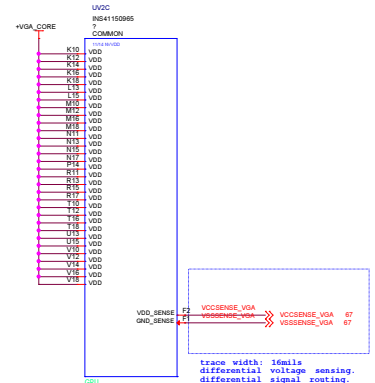
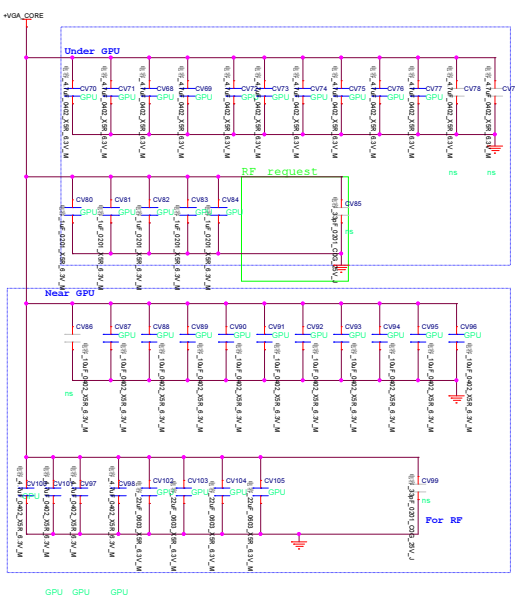
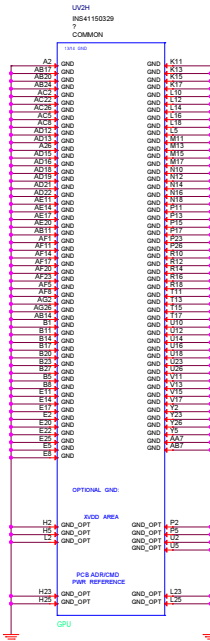
Table 7.18 GB2C-64 Package: Power Rail Filtering

Rail (GPU Ball) Name	Balls	Voltage: Current	Filtering under GPU	Filtering Near GPU
NVDD	31	Varies	2 X 4.7uF (E402) 8 X 4.7uF (E403) 1 X 330uF (P05cap) Near VR:	4 X 4.7uF (E805) 8 X 10uF (E805) 3 X 22uF (E805) 1 X 330uF (P05cap) 2 X 10uF (E805)
NVDD5	10	Varies	2 X 1uF (E402) 4 X 4.7uF (E403)	7 X 10uF (E805) 1 X 22uF (E805) 1 X 330uF (P05cap)
FBVDDQ [GPU side]¹	22	1.35V 1.5V 1.55V	2 X 1uF (E402) 1 X 10uF (E403)	10uF (E403) 3 X 22uF (E803)
FBA_PLL_AVDD	1	1.8V	2 X 0.1uF (E402 X7R)	1 X 300 bead (E402 max ESR 10 mΩ)
FB_REPLL_AVDD	1	1.8V	0.1uF (E402 X5R)	1 X 22uF (E805)
IFPAB_PLLVDD	1	1.8V	1 X 0.1uF (E402 X5R)	1 X 300 bead (E402 max ESR 10 mΩ)
GPCPLL_AVDD	2	1.8V	2 X 0.1uF (E402 X5R)	1 X 22uF (E805)
XS_PLLVDD	1	1.8V	2 X 0.1uF (E402 X5R)	1 X 4.7uF (E402)
3P_PLLVDD	1	1.8V	1 X 0.1uF (E402 X5R)	1 X 4.7uF (E402)
10V_FLLVDD	1	1.8V	1 X 0.1uF (E402 X5R)	1 X 4.7uF (E402)
IFP_OVDD	2	1.0V	2 X 0.1uF (E402 X5S)	1 X 1uF (E402)

Table 7.18 GB2C-64 Package: Power Rail Filtering (Continued)

Rail (GPU Ball) Name	Balls	Voltage: Current	Filtering under GPU	Filtering Near GPU
PEX_HQDD	14	1.8V	4 X 1uF (E402 X5R)	Near GPU: 2 X 4.7uF (E803) 2 X 10uF (E805) 1 X 22uF (E805)
PEX_PLL_HQDD	2	1.8V	1 X 0.1uF (E402)	Near GPU: 2 X 4.7uF (E803) 2 X 10uF (E805) 1 X 22uF (E805)
PEX_OVDD	6	1.0V	2 X 1uF (E402 X5R)	Near GPU: 2 X 4.7uF (E803) 2 X 10uF (E805) 1 X 22uF (E805)
1VR_MAIN	2	1.8V	2 X 0.1uF (E402)	1 X 1uF (E402)
1VR_AON	2	1.8V	2 X 0.1uF (E402)	1 X 1uF (E402)

Note:
1. Also see Section 9.2.2.10.1



Memory - Lower 32 bits

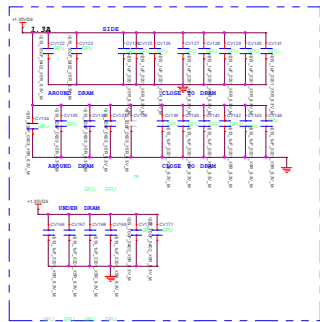
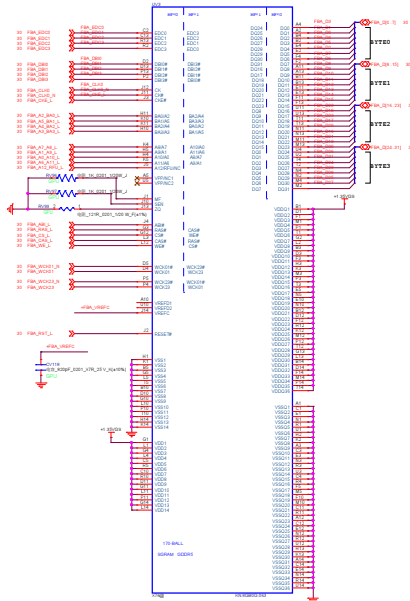
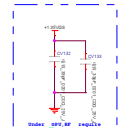
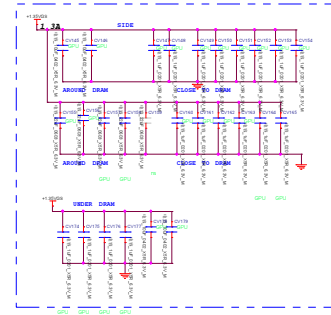
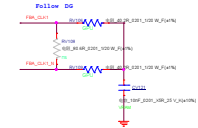
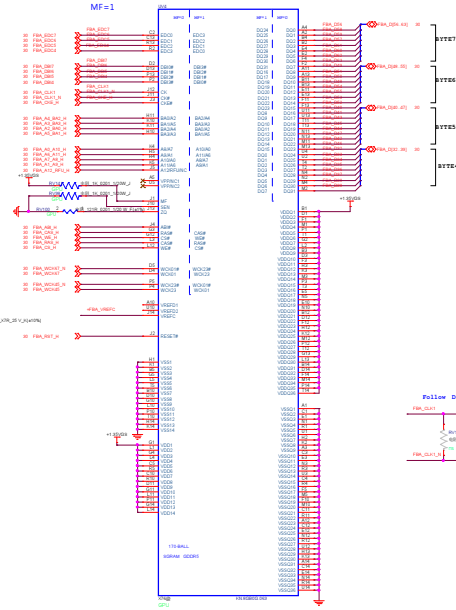
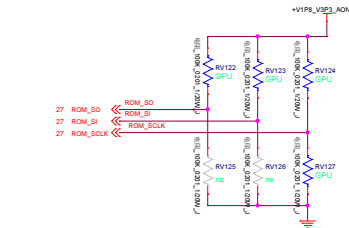
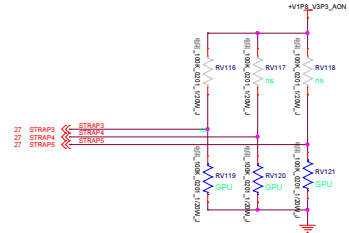
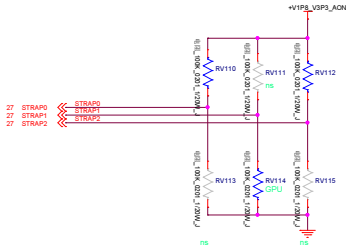


Table 9.19 DRAM-Side FBVDD/FBVDDQ Decoupling (Combined Rail)

Decoupling Capacitors			Recommended Quantity and Placement (per DRAM device).
Capacitance	Type [Size]	Quantity	Placement (by DRAM Interface Mode)
Combined FBVDD-FBVDDQ Rail			
1.0 uF	X65 [040]	10	For x32 DRAM: Under the DRAM FBVDD or FBVDDQ ball.
10 uF	X65 [0603]	4	For x16 DRAM in a "clamshell" PCB configuration: as close to DRAM periphery as possible.
1.0 uF	X65 [0402]	8	For x32 DRAM: Choose x32 interface to achieve max POR DRAM speeds. Add these additional decoupling caps under the DRAM FBVDD/Q ball; should share existing FBVDD/Q ball via if possible. See Figure 9.23 for an example.
10 uF	X65 [0603]	2	Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.
22 uF	X65 [0603]	5	For 4 GTE QMC (8 Gbps data rates): Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.

Memory - Upper 32 bits





For N17

GPU	Vendor	Manufacturer	Strap	Strap2	Strap1	Strap0
N17S-G1	Samung	K4GB0325FB-RC25	0x0	L	L	L
	Micron	MT51J256M32HF-701A	0x1	L	L	H
	Hynix	H5GC8H24JR-ROC	0x2	L	H	L
	Micron	MT51J256M32HF-701B	0x4	H	L	L
	Hynix	H5GC8H24JR-ROC	0x5	H	L	H
N17S_G0/G2	Micron	MT51J256M32HF-701B	0x9	L	M	L
	Hynix	H5GC8H24JR-R2C	0xA	L	M	H

N17S_G0/G2 follow N17S_G1 with NV confirm

FN	MFN	STRAP	Vendor
W011121854000	MT51J256M32HF-701B	0x4	Micron
W011121852000	H5GC8H24JR-ROC	0x5	Hynix
W011121870000	K4GB0325FB-RC28	0x0	Samung

Physical Strapping pin	Power Rail	RAM_CFG[3]	RAM_CFG[0x02]	RAM_CFG[1]	RAM_CFG[0x00]
STRAP0		L		L	
STRAP1		H		L	
STRAP2		L		L	

SMBUS ALT ADDR
0 0x6E (Default)
1 0x6C (Multi-GPU usage)

DEVID SEL
0 (Default)
1

PCIE CFG
0 (Default)
1

VGA DEVICE
0 3D Device (Class Code 302h)
1 VGA Device (Default)

Physical Strapping pin	Power Rail	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SCLK	H				
ROM_S1	H	Disable	Disable	Disable	Disable
ROM_S0	H				

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0	(0x0000)
L	L	H	1	(0x0001)
L	H	L	2	(0x0002)
L	H	H	3	(0x0003)
H	L	L	4	(0x0004)
H	L	H	5	(0x0005)
H	H	L	6	(0x0006)
H	H	H	7	(0x0007)
L	L	M	8	(0x0008)
L	M	L	9	(0x0009)
L	M	H	10	(0x000A)
L	H	M	11	(0x000B)
M	L	L	12	(0x000C)
M	L	H	13	(0x000D)


Table 5. N17S-G0/G2 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mb/32 512Mb/16	1.35V	Hynix	H5GC8H24JR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready

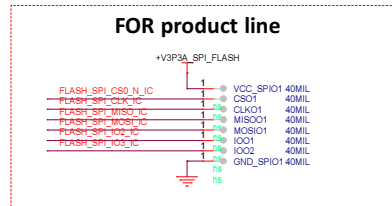
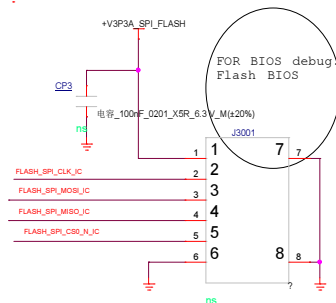
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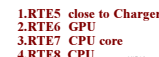
- For N17S-G0/G2, the maximum allowable memory case temperature is 85 °C.
- N17S-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) will also use the memory configurations in Table 4 for N17S-G1.



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ODD

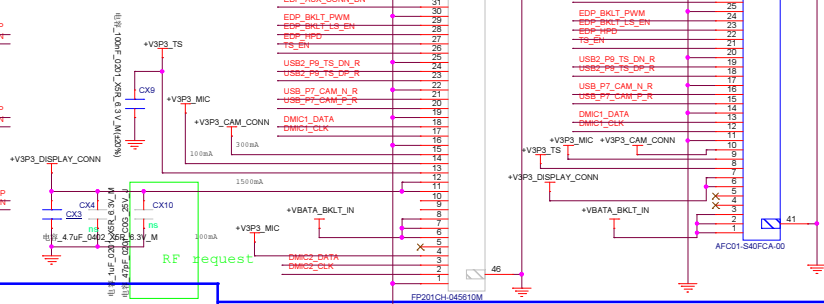
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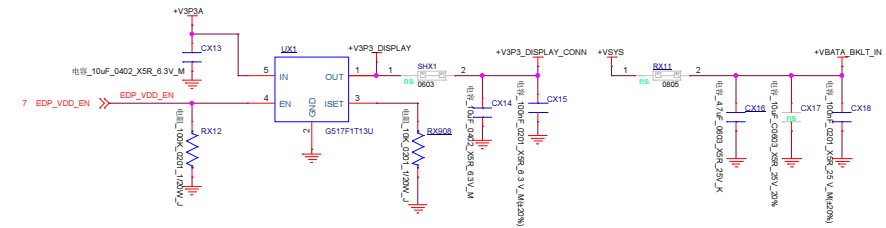
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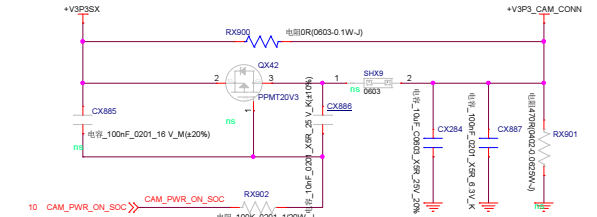
eDP & CAM & DMIC & Touch Panel CONN



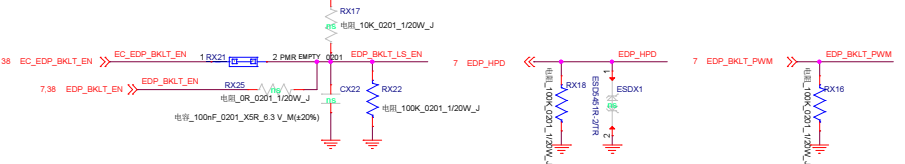
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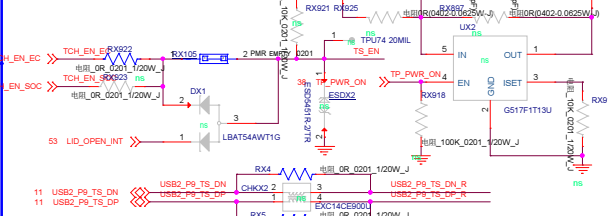
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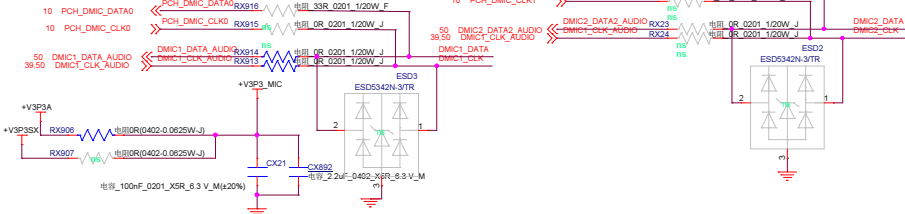
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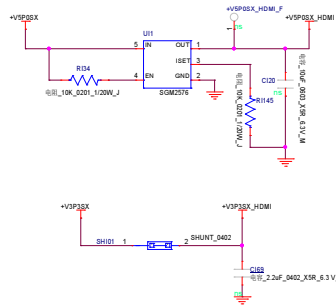
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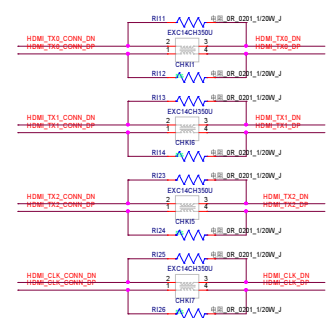
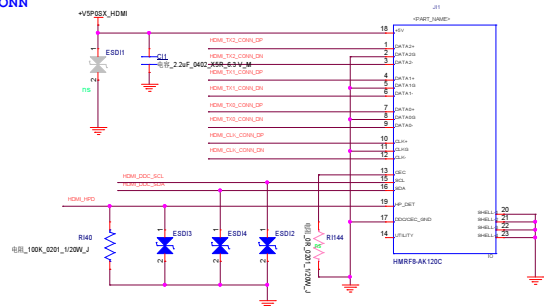
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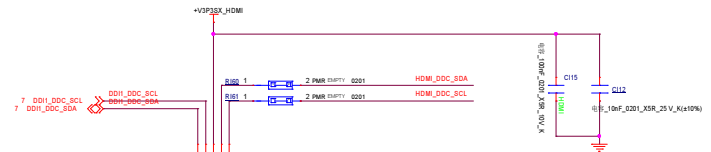
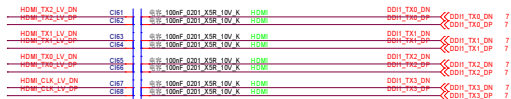
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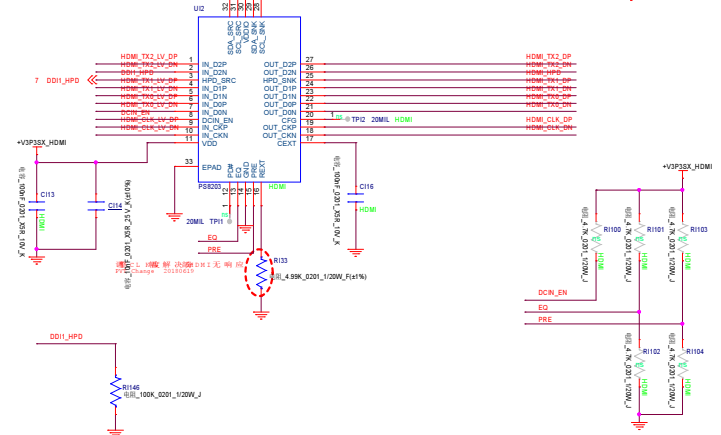
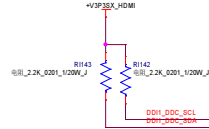
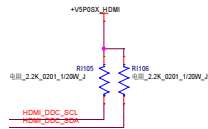
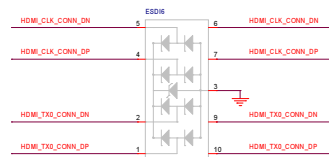
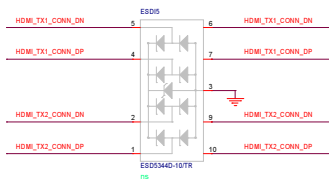
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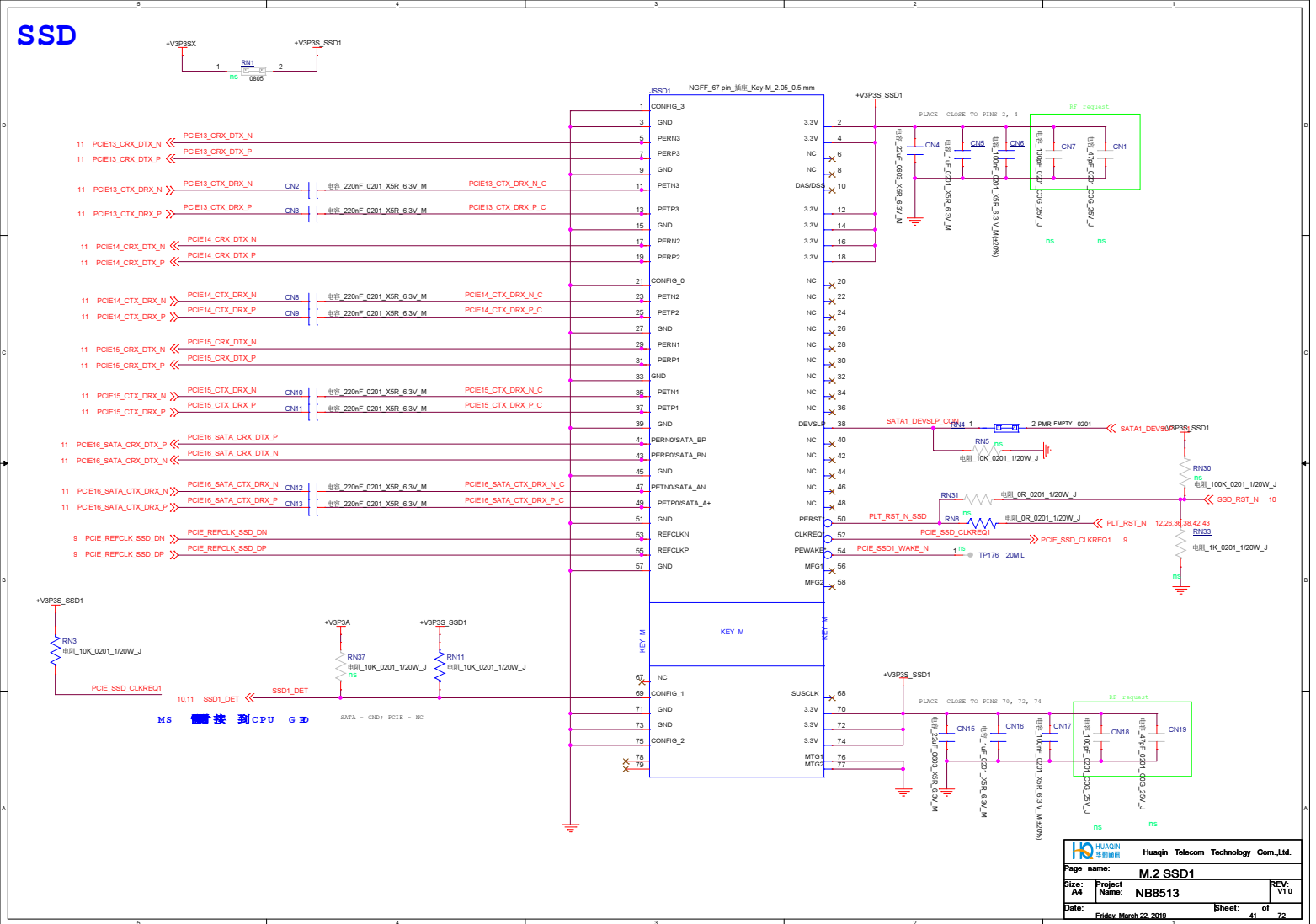
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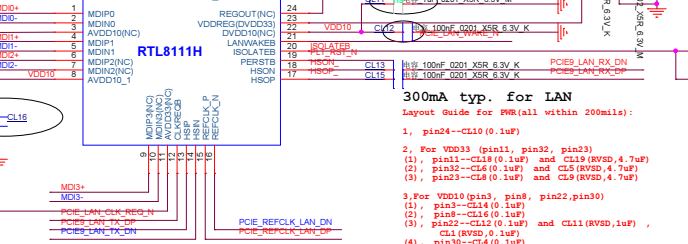
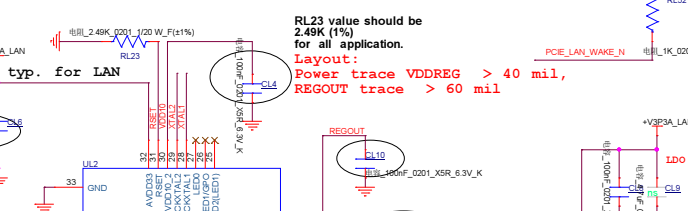
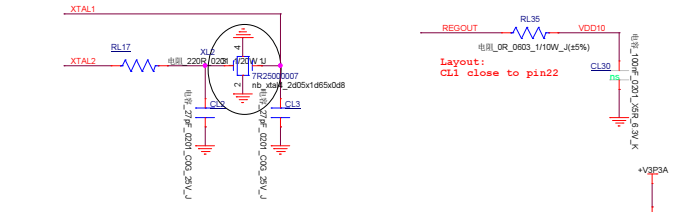
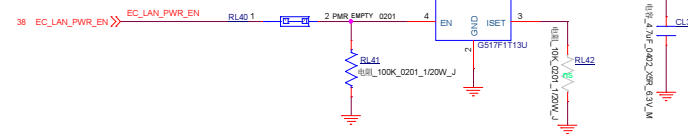
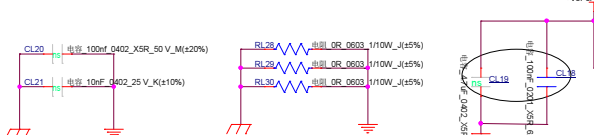
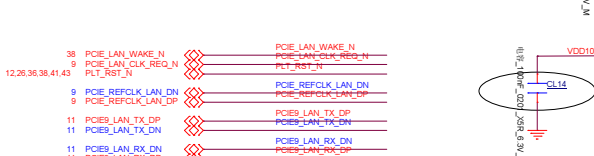
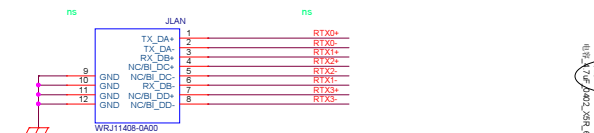
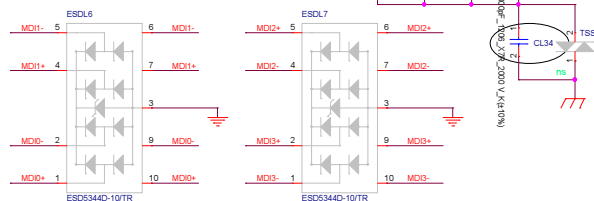
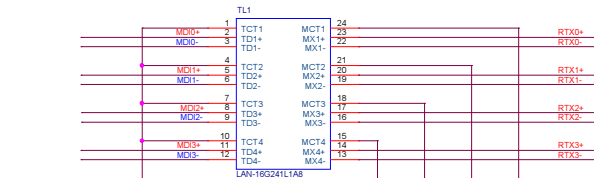


ESD



SSD





Support AC S5 S4 LAN WAKE S3 LAN WAKE

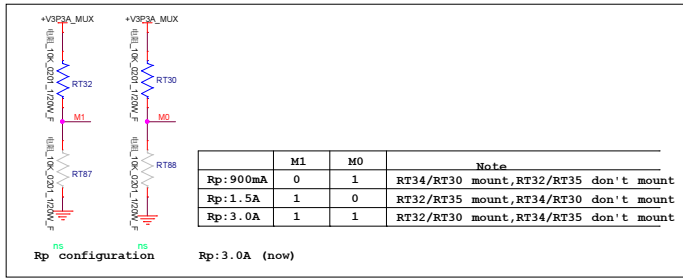
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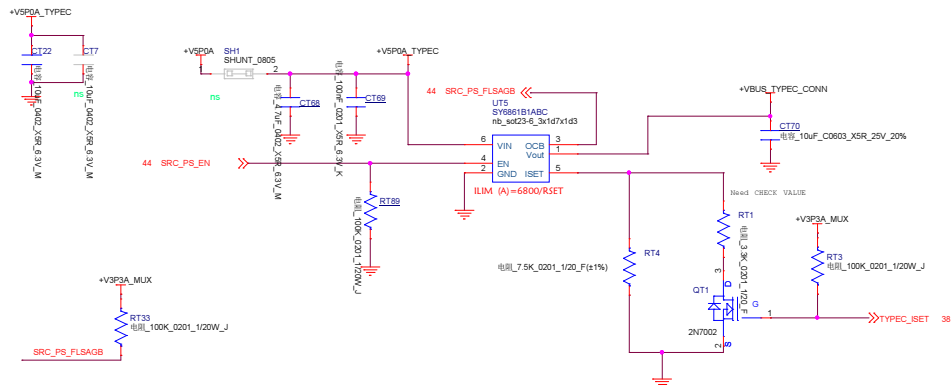
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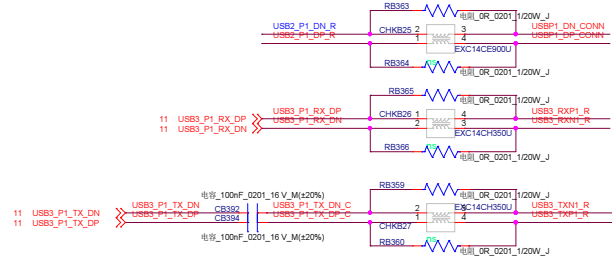
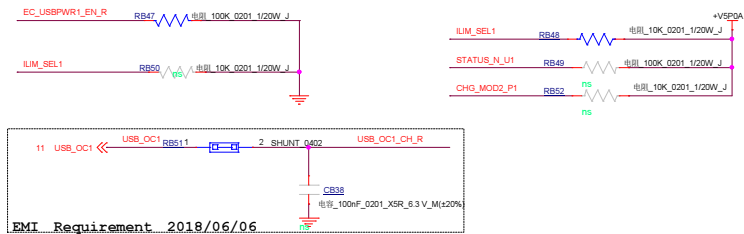
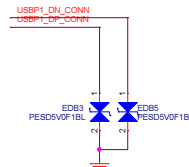
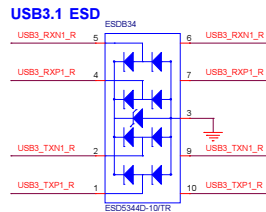
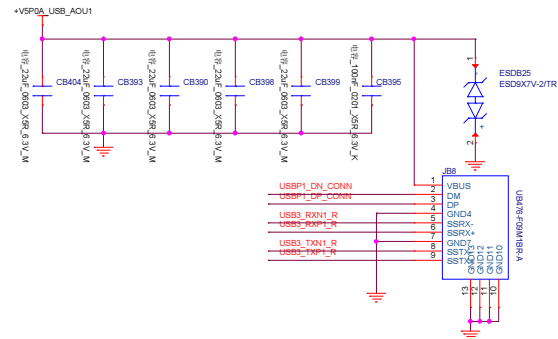
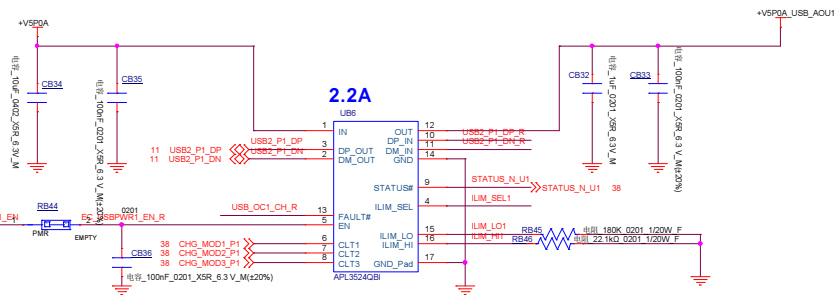
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Layout: CL1 close to pin22


Layout: CL1 close to pin22
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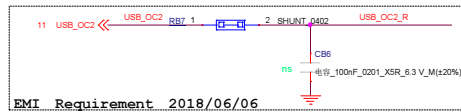
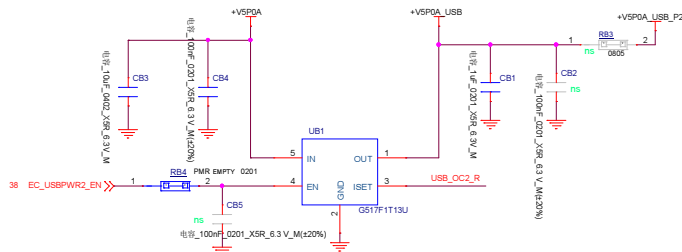
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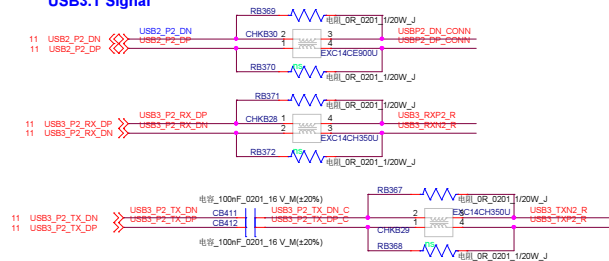




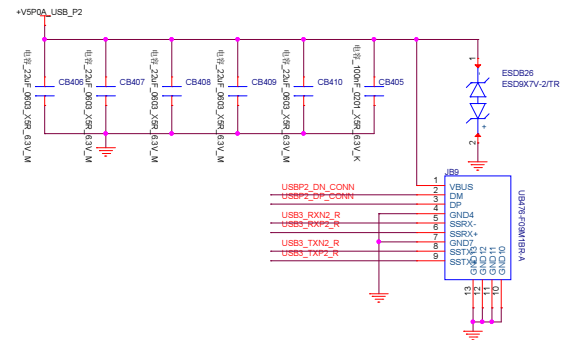
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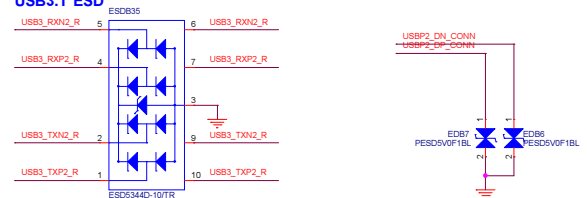
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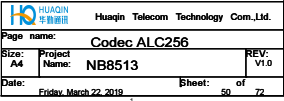
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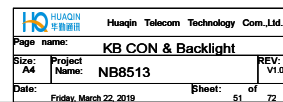
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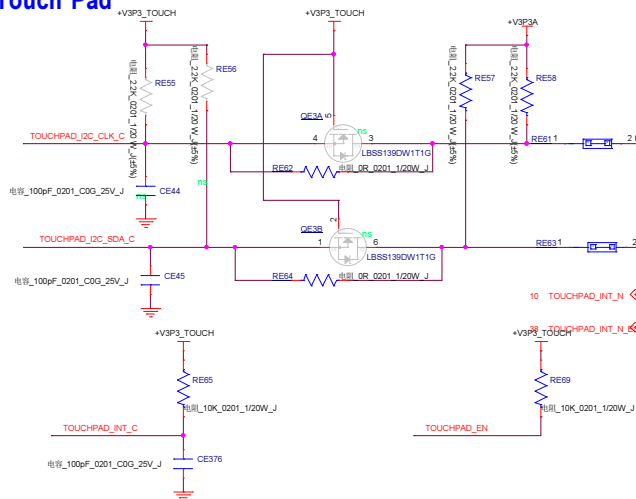
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1.8V \pm 5%	1.8V \pm 5%	support
1.8V \pm 5%	1.5V \pm 5%	support
1.8V \pm 5%	3.3V \pm 10%	Not support



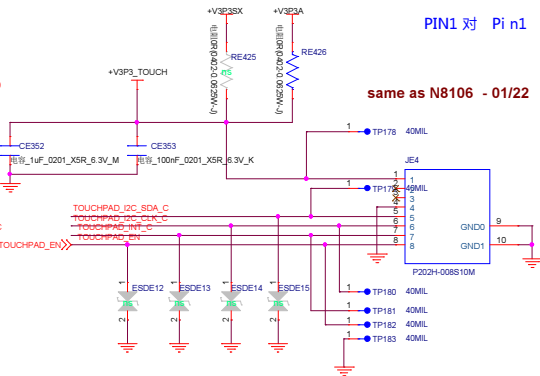
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Touch Pad



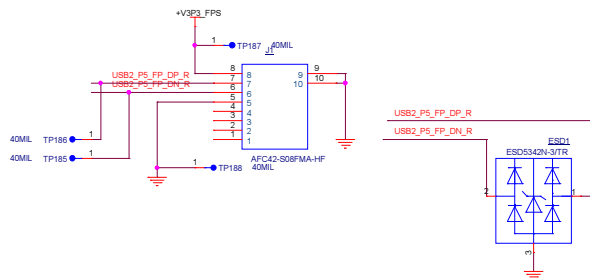
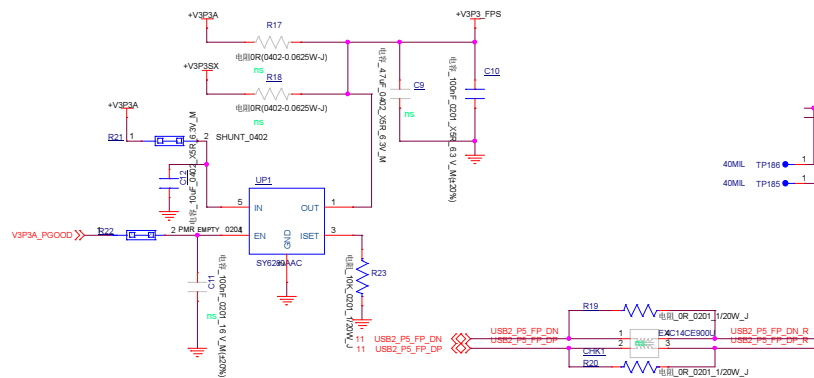
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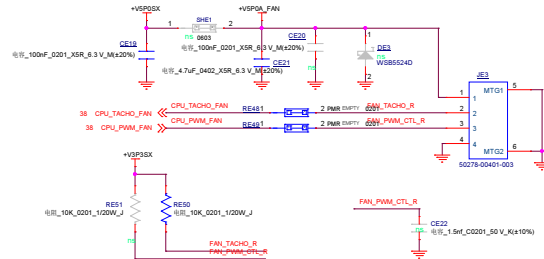


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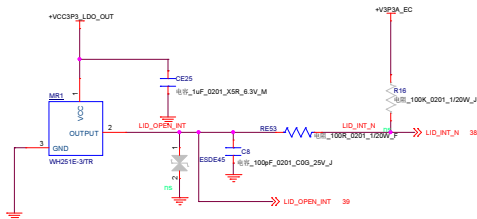
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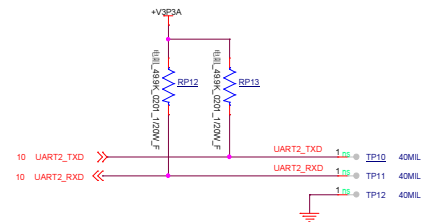
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确认 P 线顺序



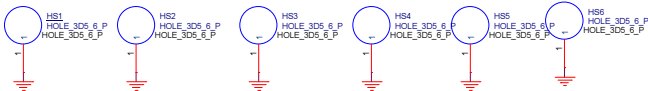




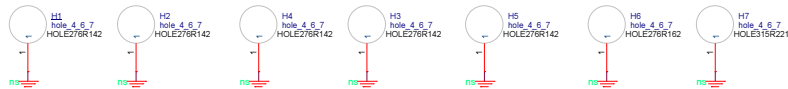
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Need add HQ CODE and Stuff

螺母元件



Thermal



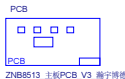
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CPU & GPU Boss

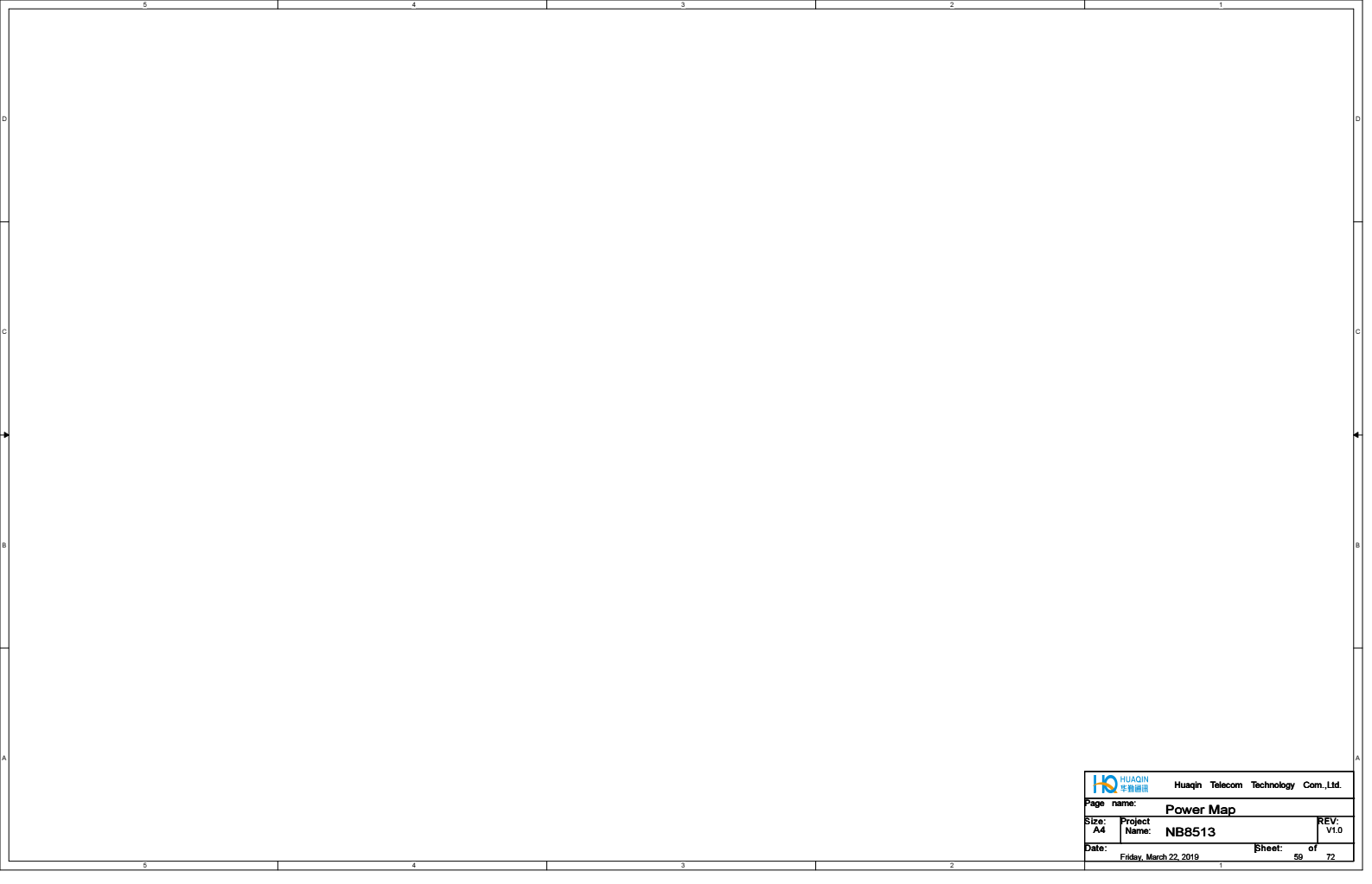



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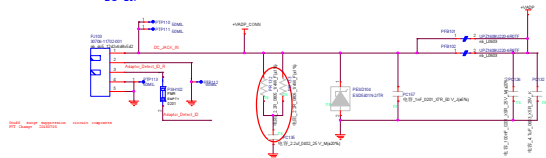
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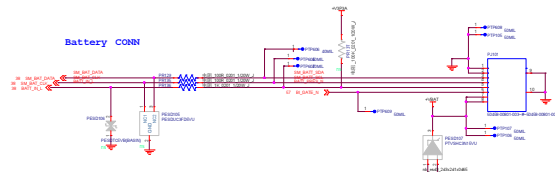


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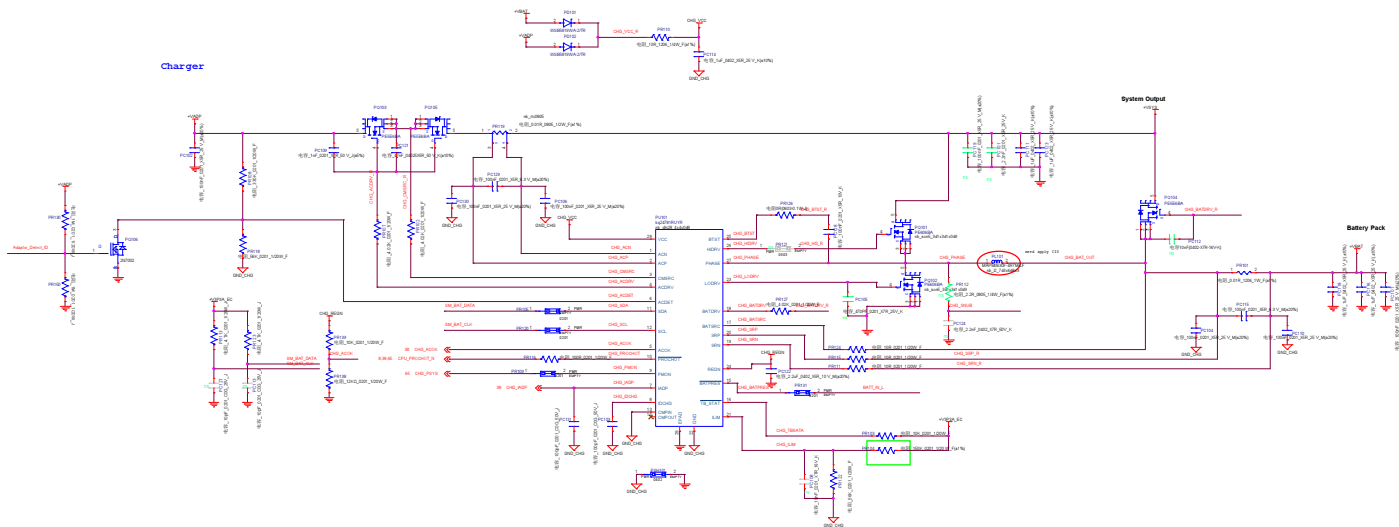
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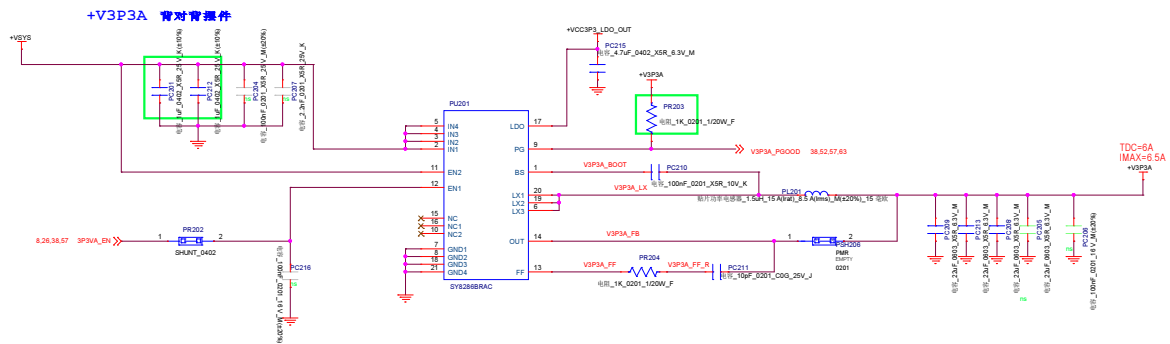


Battery CONN

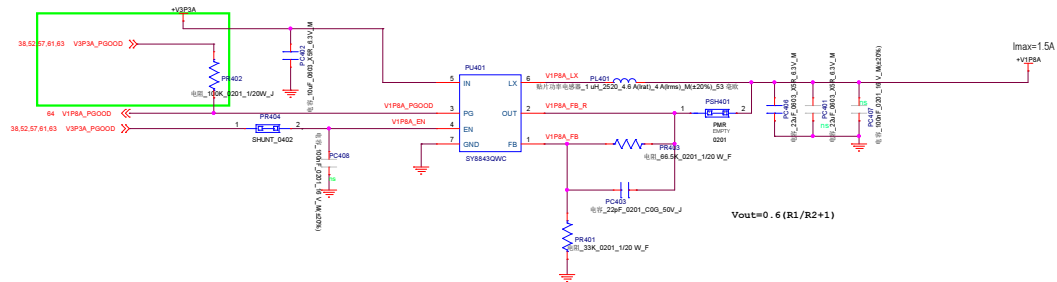


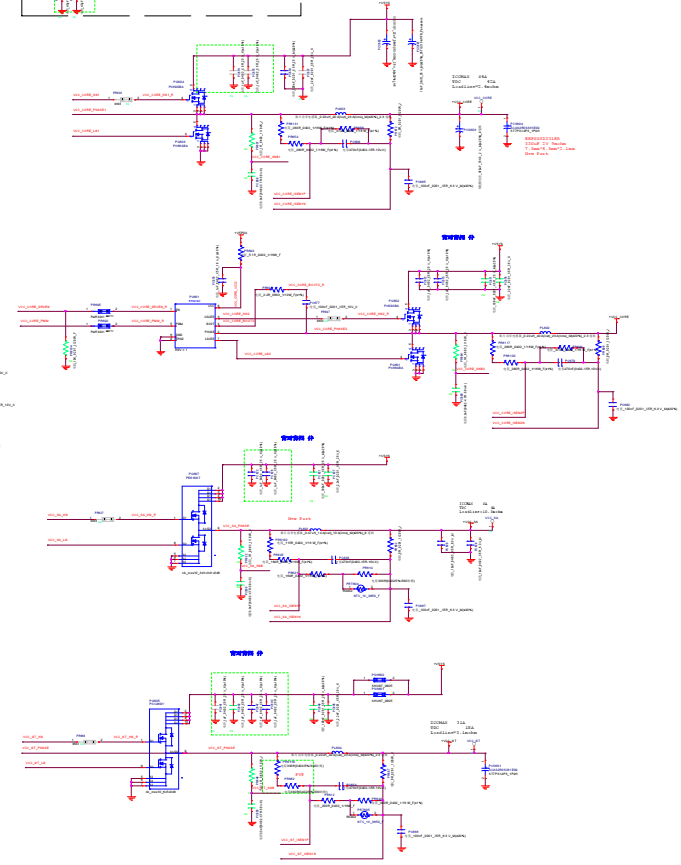
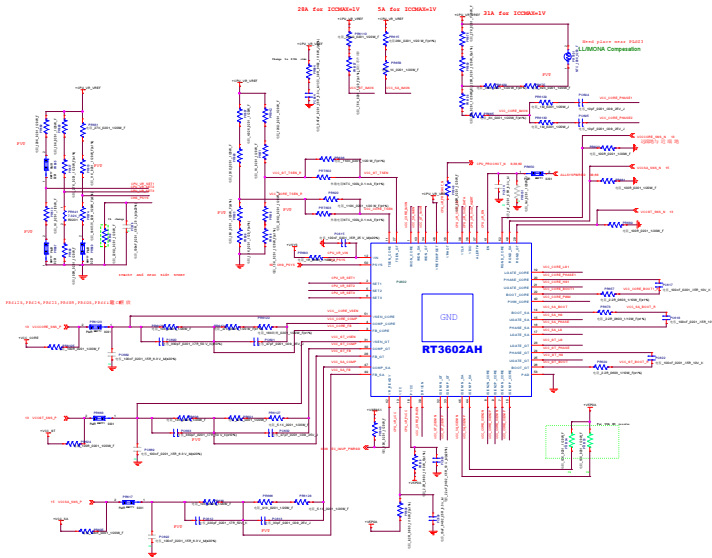
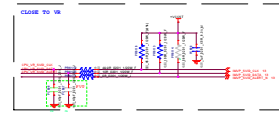
Charger





+V1P8A



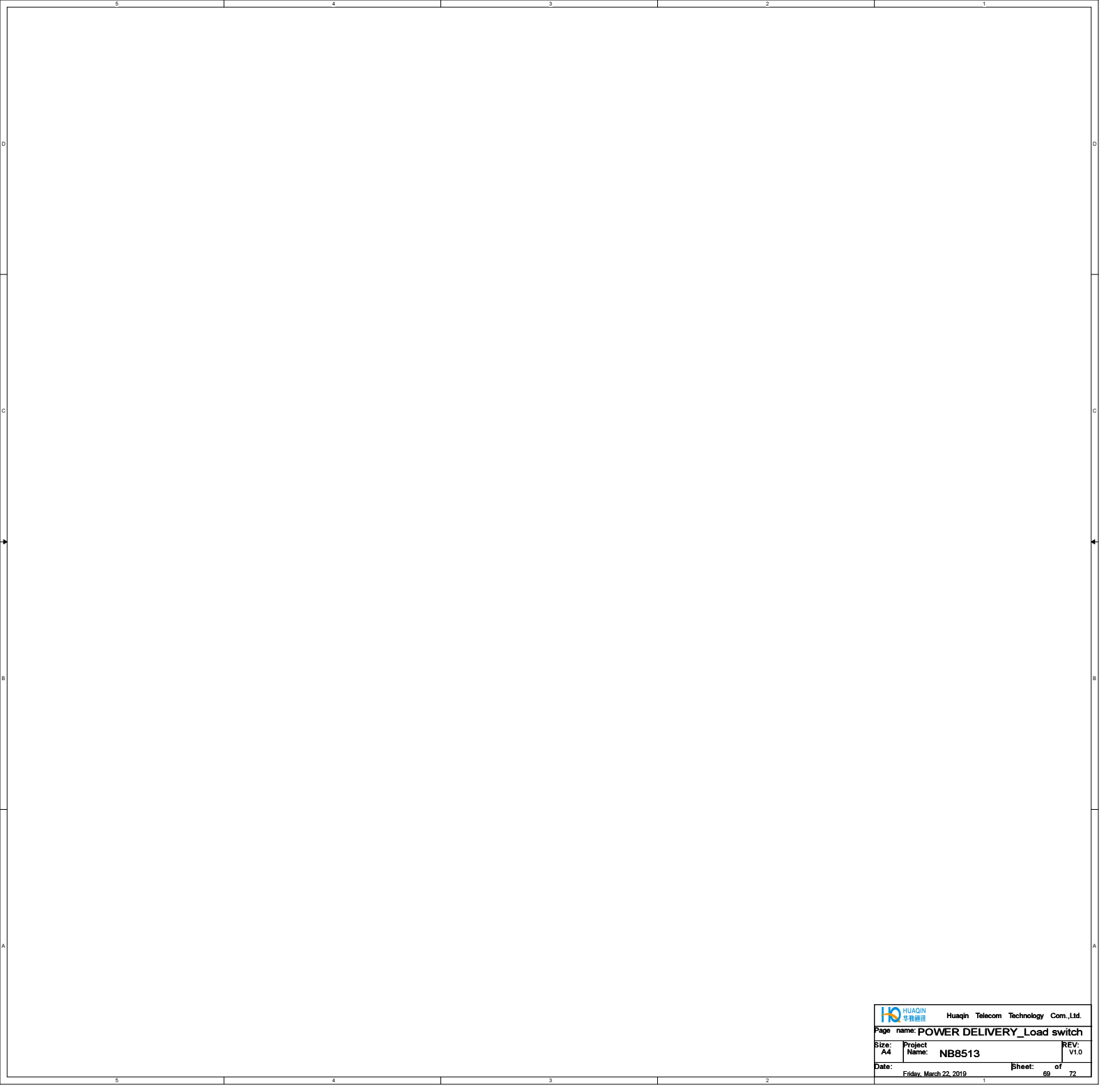


	CML Part	CML Base	WHL
ICCMAX[A]	85	70	70
IPL2[A]	58	48	48
DC/AC LL[mQ]	1.8	1.8	1.8
GT ICCMAX [A]	31	31	31
GT IPL2[A]	18	18	18
GT DC/AC LL[mQ]	3.1	3.1	3.1
SA ICCMAX[A]	6	6	6
SA DC/AC LL[mQ]	10.3	10.3	10.3
IPL2 [V]	84	51	51
IPL2 [V]	90	52	71
IPL2 [V]	90	52	71

[illegible][illegible][illegible]

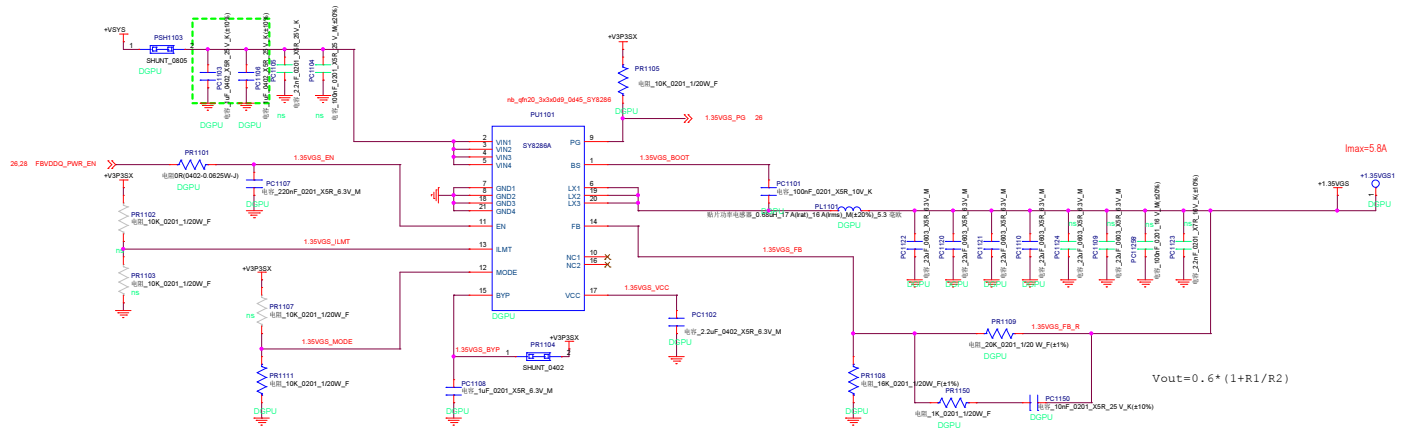
							Six transactions
tCPU26	All	CPU	PLT	10	65	us	11 CPU_C10_GATE# de-assertion to VCCSTG stable Note: CPU_C10_GATE# de-assertion to VCCSTG also needs to meet max: 65us on cold boot
tCPU27	All	CPU	PLT	10	240	us	11 CPU_C10_GATE# de-assertion to VCCG0 stable
tCPU28a	All	CPU	PLT		200	us	36 SLP_S3# assertion to VCCSTG_PWRGD low to VCCSTG
tCPU28b	All	CPU	PLT	0		us	37.38 VCCSTG_PWRGD low to VCCSTG

[illegible][illegible][illegible]




Update according to vendor--2018/9/19

背对背组件



ILMT=Low	6.7	7.8	8.9	A
ILMT=Floating	9.3	10.6	11.9	A
ILMT=High	12	13.3	14.8	A



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